

# LCFC Confidential


## BY511/BY710 M/B Schematics Document

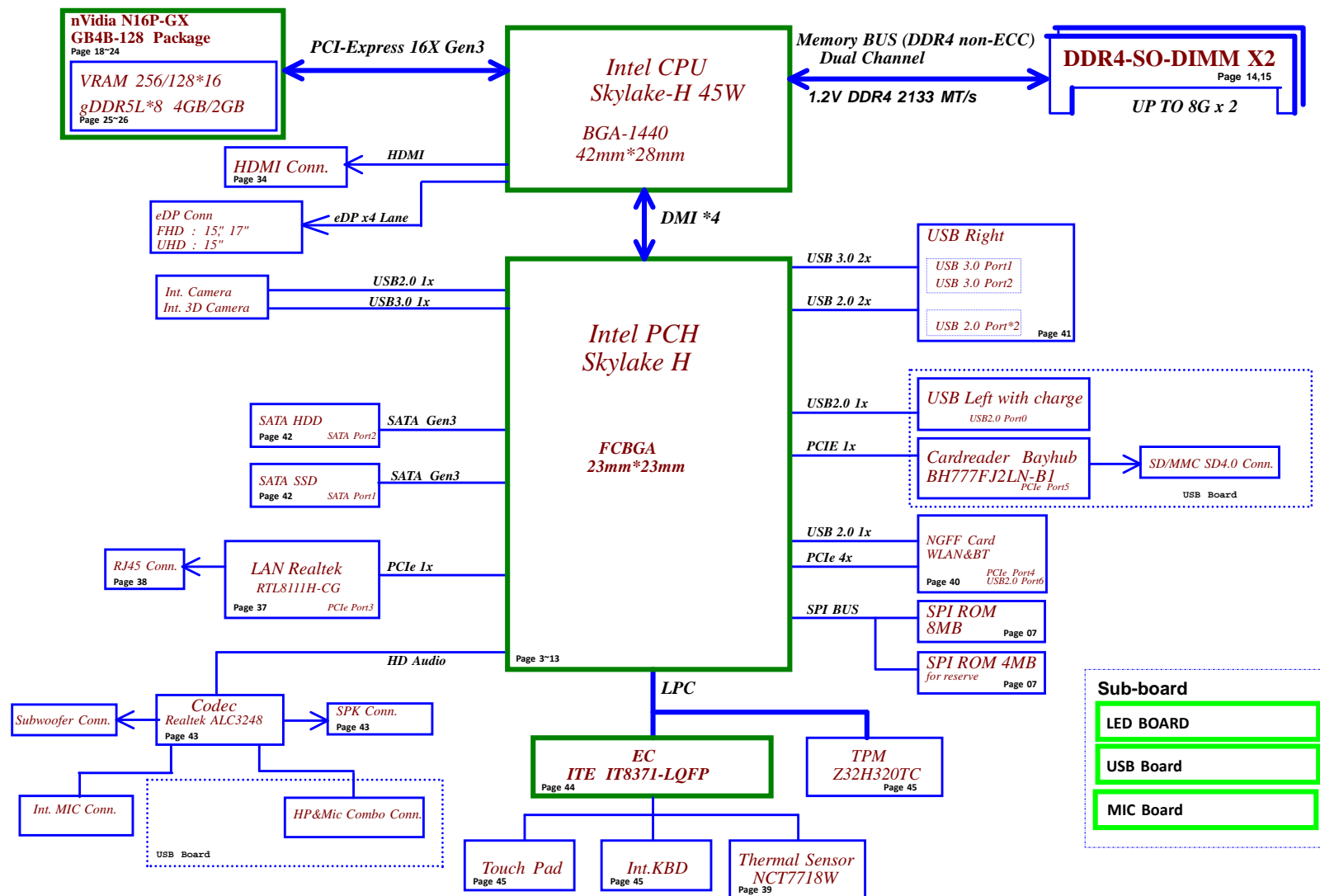
Intel Skylake H-Processor with DDR4 + NV N16P-GX GPU

MB NMA541

2015-07-31

REV:1.0

Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/02/26	Deciphered Date	2016/02/26	Cover Page		
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Voltage Rails ( 0 --> Means ON , X --> Means OFF )

Power Plane / State					
	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS +1.5VS +1.2VS +1.05VS  +0.6VS CPU_CORE  +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	0	0	0	0	0
S3	0	0	0	0	X
S3 Battery only	0	0	0	0	X
S5 S4/AC Only	0	0	0	X	X
S5 S4 Battery only	0	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB 2.0 Port table

Port	Function
1	RIGHT USB 2.0 (AOU)
2	LEFT USB 3.0 w/ 2.0
3	LEFT USB 3.0 w/ 2.0
4	
5	Touch Screen
6	Camera
7	
8	
9	
10	
11	Buletooth
12	
13	
14	

PCIE 3.0 Port table

Port	Function
1	
2	SD 4.0 Card Reader
3	WLAN
4	LAN
5	
6	
7	
8	
9	M.2 SSD 4Lanes PCIe
10	M.2 SSD 4Lanes PCIe
11	M.2 SSD 4Lanes PCIe
12	M.2 SSD 4Lanes PCIe
13	
14	
15	
16	

SATA 3.0 Port table

Port	Function
1	M.2 SSD SATA Gen3
2	HDD SATA Gen3
3	
4	

USB 3.0 Port table

Port	Function
1	LEFT USB 3.0 w/ 2.0
2	LEFT USB 3.0 w/ 2.0
3	
4	
5	
6	3D Camera
7	
8	

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
AOAC@	AOAC support part
GIGA@	GIGA LAN Part
ME@	ME part(connector, hole)
RANKA@	For VRAM RankA part
RANKB@	For VRAM RankB part
OPT@	For GPU part
TS@	For support touch panel sku part
TPM@	For support TPM sku part
U31@	For support USB re-driver part
3D@	For support 3D camera sku part
H4@	Hynix 256Mx16 VRAM part
M4@	Micron 256Mx16 VRAM part
S4@	Samsung 256Mx16 VRAM part
S4GX4@	Samsung 256Mx16 VRAM x4pcs sku
H4GX4@	Hynix 256Mx16 VRAM x4pcs sku
M4GX4@	Micron 256Mx16 VRAM x4pcs sku
CD@	Cost down part
H4GX8@	Hynix 256Mx16 VRAM x8pcs sku
M4GX8@	Micron 256Mx16 VRAM x8pcs sku
S4GX8@	Samsung 256Mx16 VRAM x8pcs sku

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address

EC SM Bus2 address

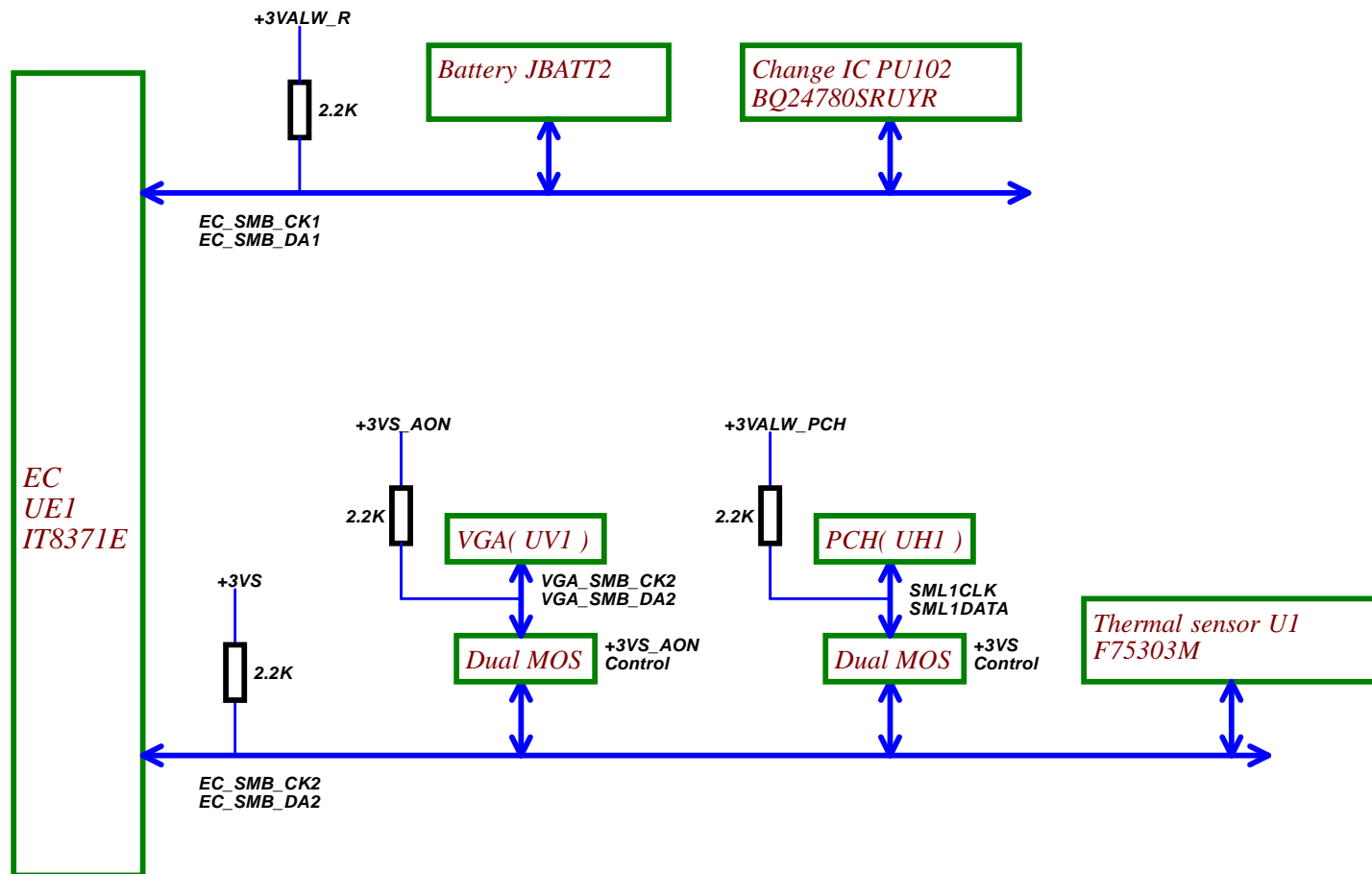
PCH SM Bus address


Device	Address
Smart Battery	0X16
Charger	0001 0010 b

Device	Address
Thermal Sensor NCT7718W	1001_100xb
VGA	0x41(default)
PCH	need to update

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

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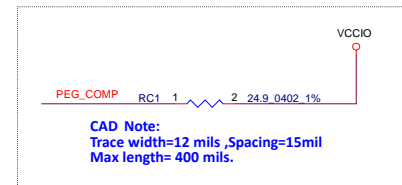
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[24] PCIE\_CRX\_GTX\_N[0..15]

[24] PCIE\_CRX\_GTX\_P[0..15]

PCIE\_CTX\_C\_GRX\_N[0..15] [24]

PCIE\_CTX\_C\_GRX\_P[0..15] [24]







HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK

[35] HDMI\_TX2+  
[35] HDMI\_TX2-  
[35] HDMI\_TX1+  
[35] HDMI\_TX1-  
[35] HDMI\_TX0+  
[35] HDMI\_TX0-  
[35] HDMI\_TXC+  
[35] HDMI\_TXC-

HDMI\_TX2+  
HDMI\_TX2-  
HDMI\_TX1+  
HDMI\_TX1-  
HDMI\_TX0+  
HDMI\_TX0-  
HDMI\_TXC+  
HDMI\_TXC-

K36  
K37  
J35  
J34  
H37  
H36  
J37  
J38  
DDI1\_TXP[0]  
DDI1\_TXN[0]  
DDI1\_TXP[1]  
DDI1\_TXN[1]  
DDI1\_TXP[2]  
DDI1\_TXN[2]  
DDI1\_TXP[3]  
DDI1\_TXN[3]

D27  
E27  
DDI1\_AUXP  
DDI1\_AUXN

H34  
H33  
F37  
G38  
F34  
F35  
E37  
E36  
DDI2\_TXP[0]  
DDI2\_TXN[0]  
DDI2\_TXP[1]  
DDI2\_TXN[1]  
DDI2\_TXP[2]  
DDI2\_TXN[2]  
DDI2\_TXP[3]  
DDI2\_TXN[3]

F26  
E26  
DDI2\_AUXP  
DDI2\_AUXN

C34  
D34  
B36  
B34  
F33  
E33  
C33  
B33  
DDI3\_TXP[0]  
DDI3\_TXN[0]  
DDI3\_TXP[1]  
DDI3\_TXN[1]  
DDI3\_TXP[2]  
DDI3\_TXN[2]  
DDI3\_TXP[3]  
DDI3\_TXN[3]

A27  
B27  
DDI3\_AUXP  
DDI3\_AUXN

4 OF 14

SKYLAKE-H-CPU\_BGA1440

SKYLAKE\_HALO

BGA1440

EDP\_TXP[0]  
EDP\_TXN[0]  
EDP\_TXP[1]  
EDP\_TXN[1]  
EDP\_TXP[2]  
EDP\_TXN[2]  
EDP\_TXP[3]  
EDP\_TXN[3]

EDP\_AUXP  
EDP\_AUXN

EDP\_DISP\_UTIL

EDP\_RCOMP

PROC\_AUDIO\_CLK  
PROC\_AUDIO\_SDI  
PROC\_AUDIO\_SDO

D29  
E29  
F28  
E28  
B29  
A29  
B28  
C28  
CPU\_EDP\_TX0+  
CPU\_EDP\_TX0-  
CPU\_EDP\_TX1+  
CPU\_EDP\_TX1-  
CPU\_EDP\_TX2+  
CPU\_EDP\_TX2-  
CPU\_EDP\_TX3+  
CPU\_EDP\_TX3-

C26  
B26  
CPU\_EDP\_AUX  
CPU\_EDP\_AUX#

A33

D37

COMPENSATION PU FOR eDP

CAD Note:Trace width=20 mils ,Spacing=25mil,  
Max length=100 mils.

G27  
G25  
G29  
PROC\_AUDIO\_CLK\_CPU  
PROC\_AUDIO\_SDO\_CPU  
PROC\_AUDIO\_SDI\_CPU\_R

20\_0402\_1% 1 2 RC180

Place near CPU.

Need create 5% P/N

RH762  
33\_0402\_5%

CH264  
10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

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10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

10P\_0402\_50V8J

1 2

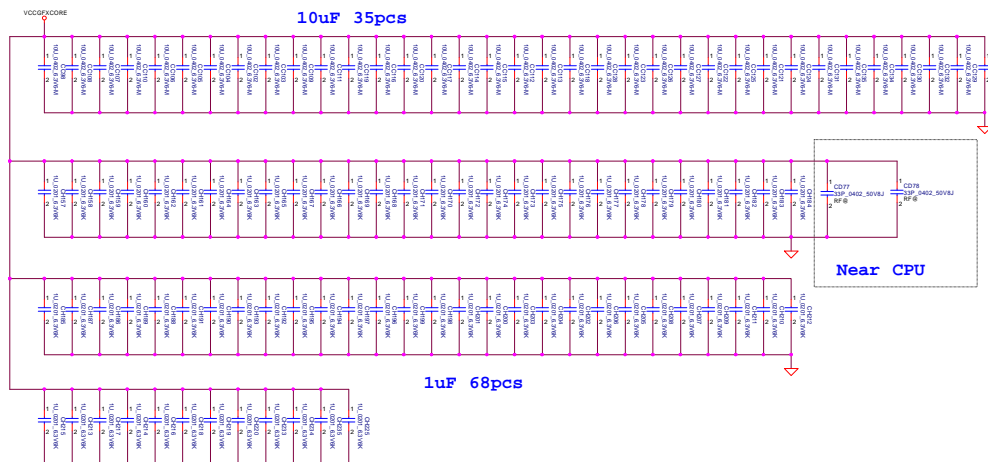
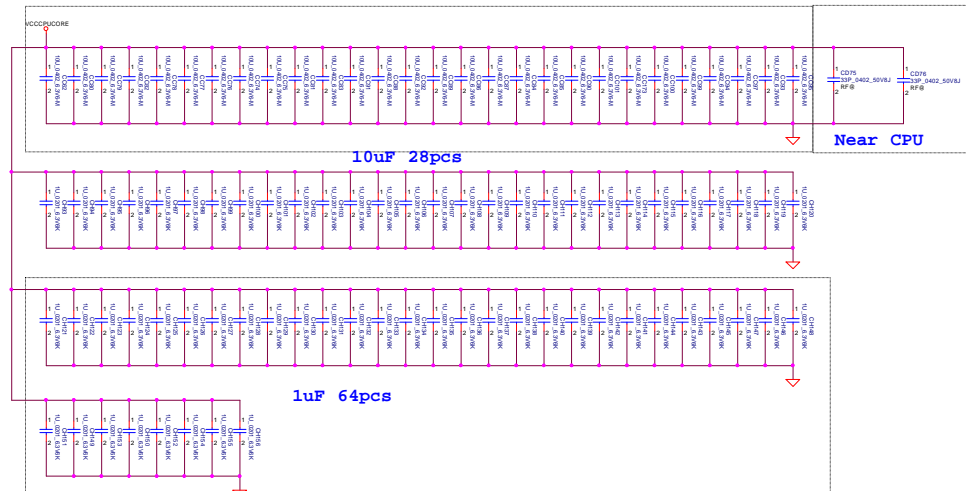
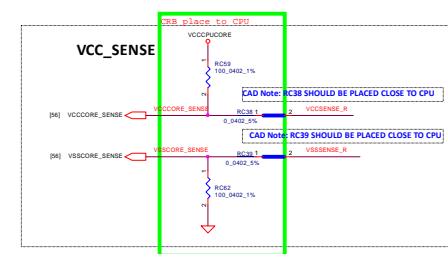
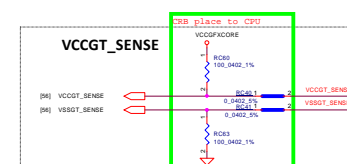
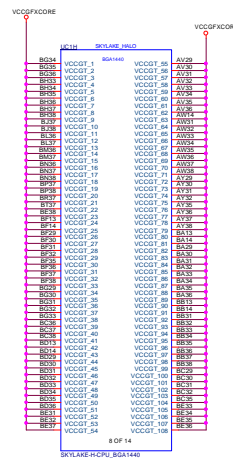
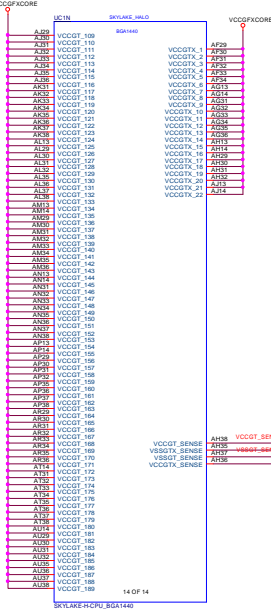
10P\_0402\_50V8J



1 2

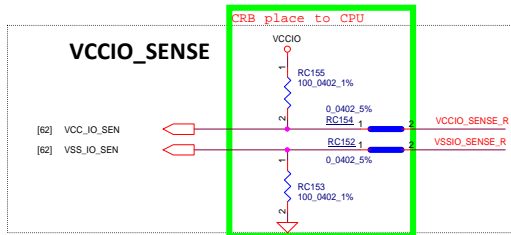
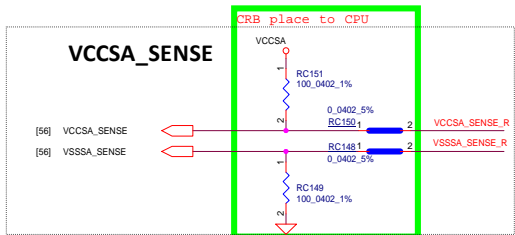
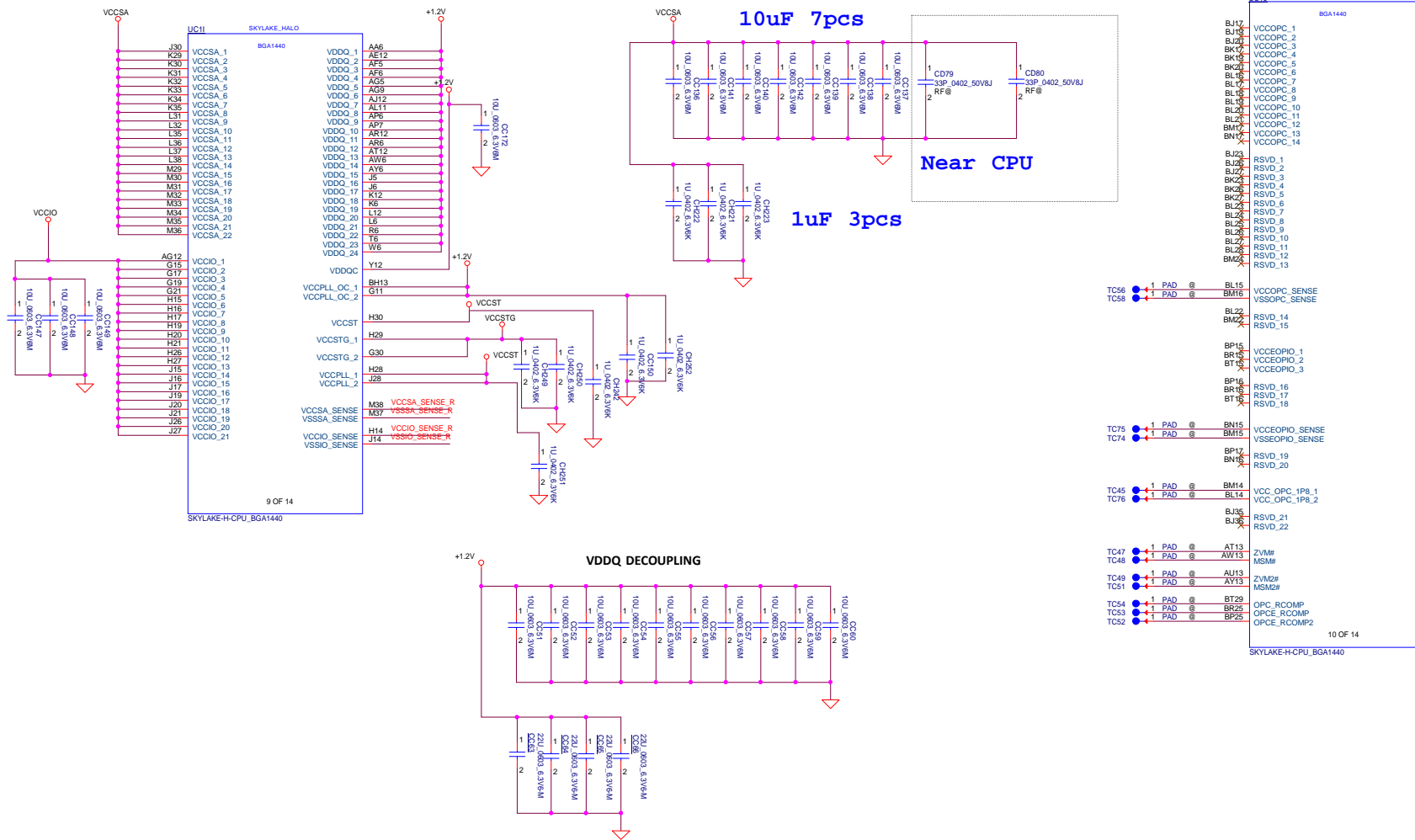
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Title		CPU (4/7) eDP, DDI	
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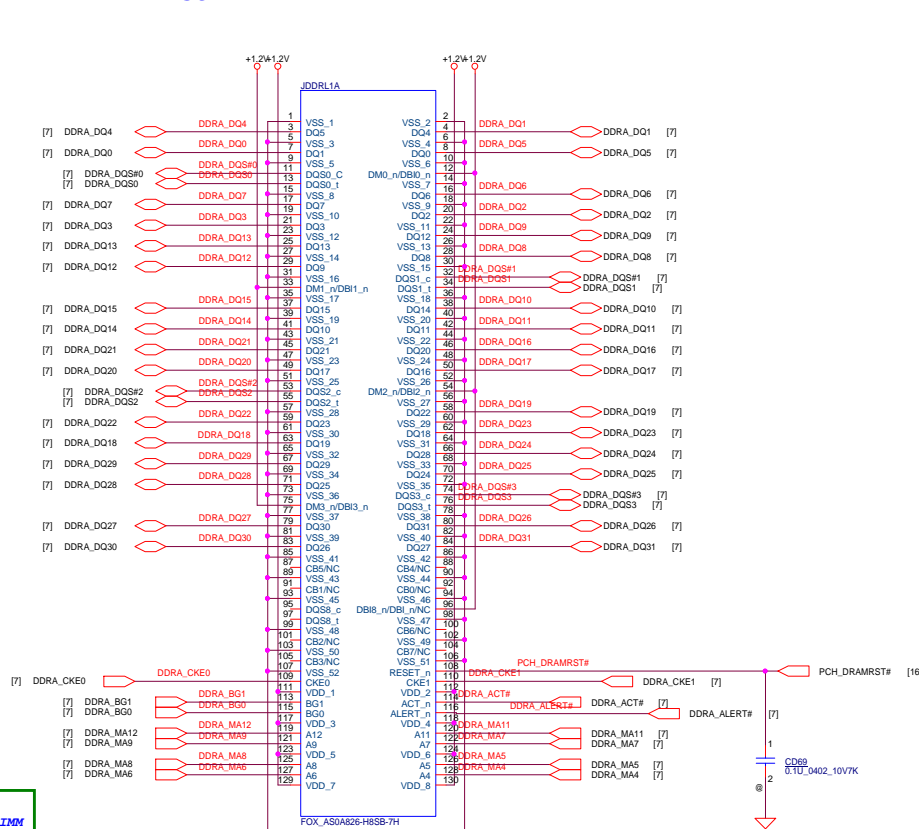




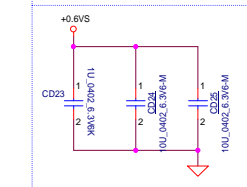
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Doc ID	Document Number	B7511/B7170	
Rev	Rev	01 06	



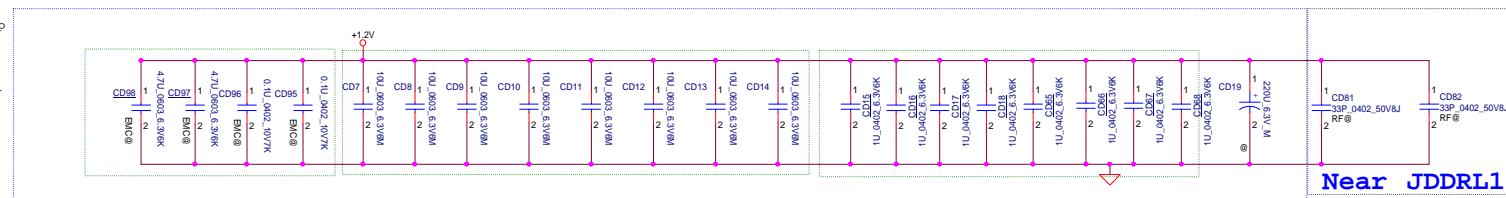
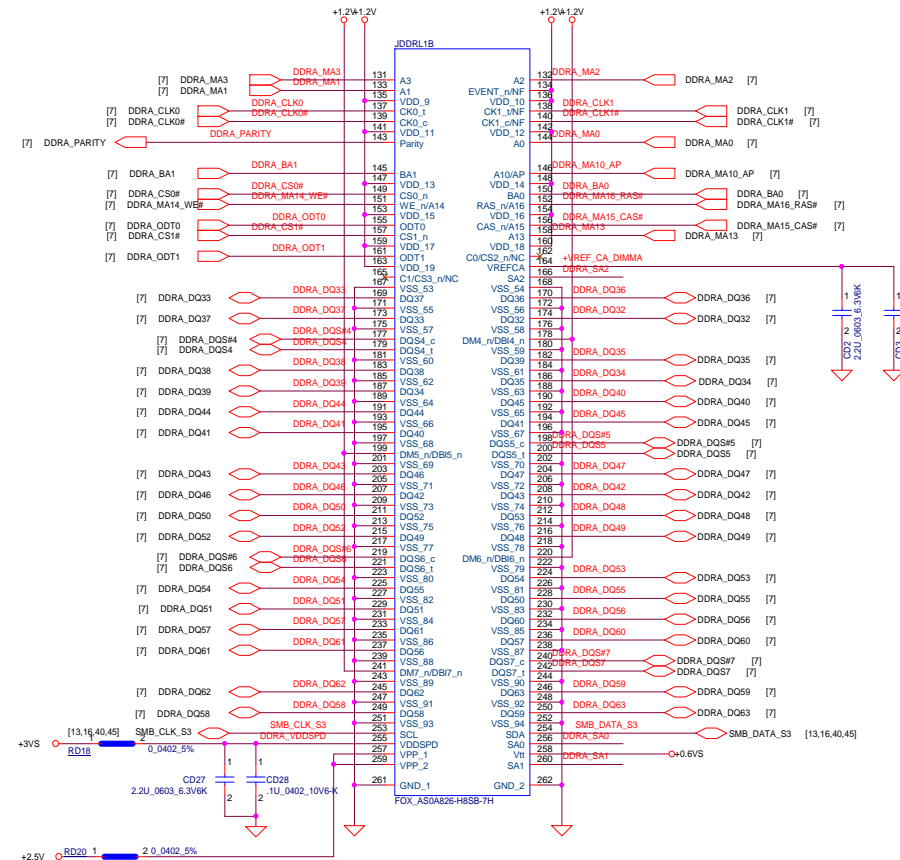
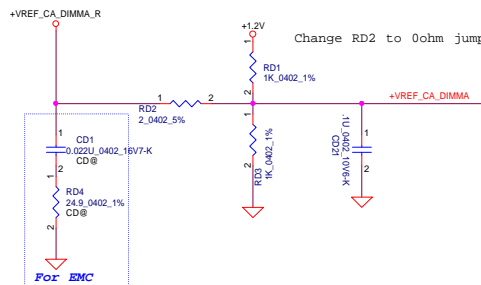



**DDR4 SO-DIMM A**

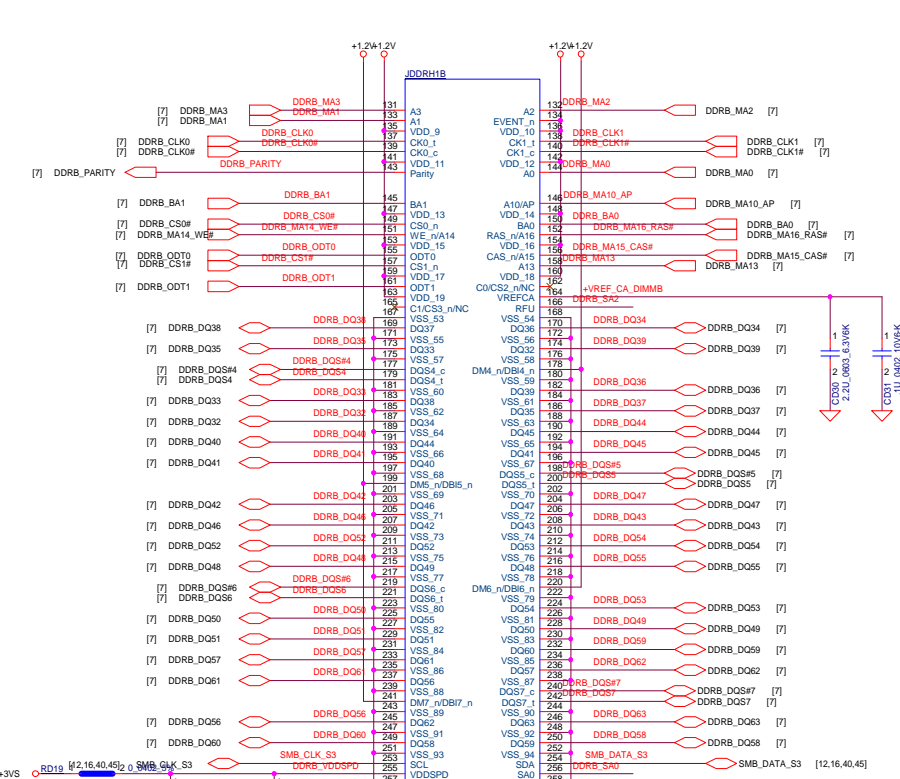
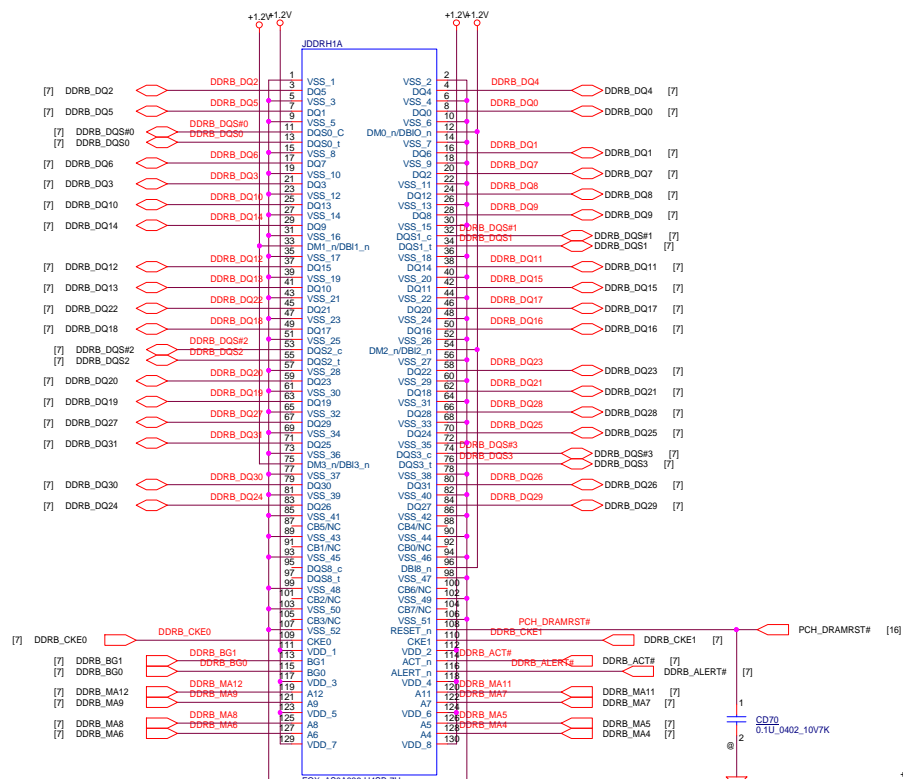
SPD Address = 0H



**Note:**  
VREF trace width:20 mils at least  
Spacing:20mils to other signal/planes  
Place near DIMM socket



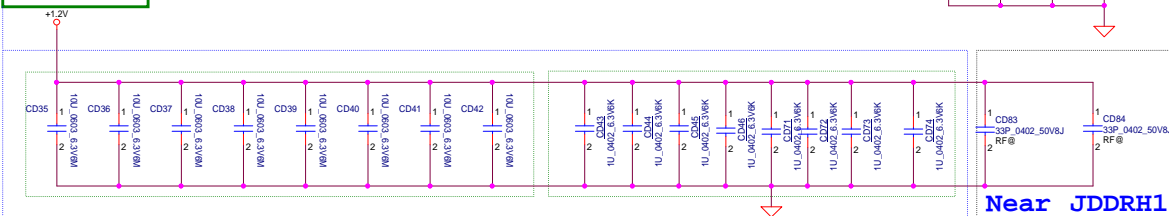
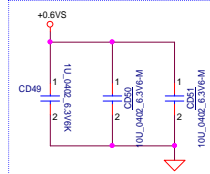
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**DDR4 SO-DIMM B**

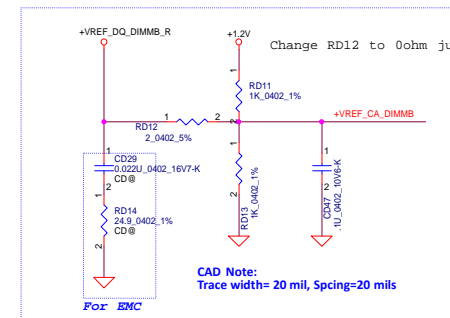
SPD Address = 2H

Layout Note:  
Place near D


Layout Note:  
Place near DIMM



Near JDDRH1



CAD Note:  
Trace width= 20 mil, Spacing=20 mils

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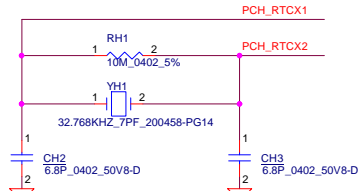
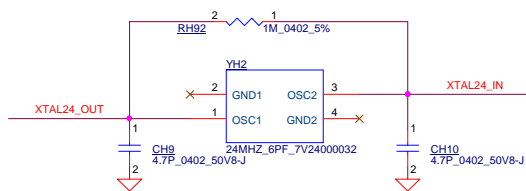
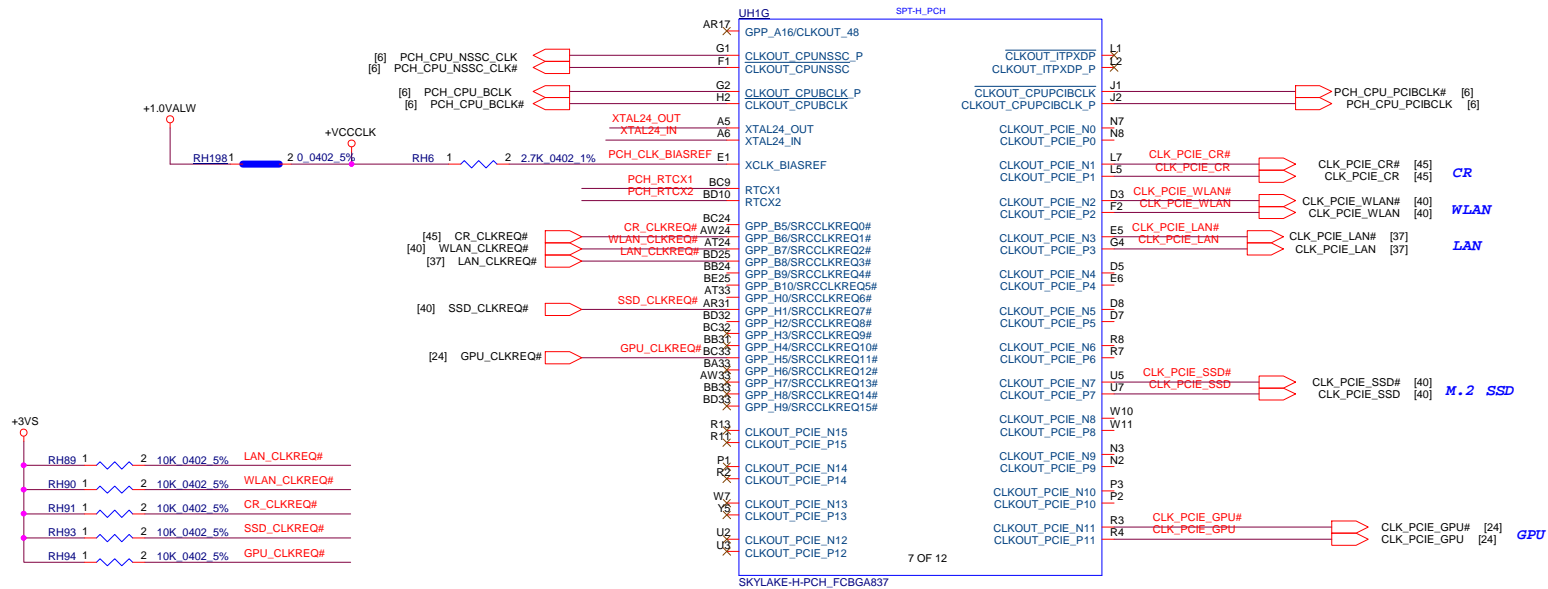


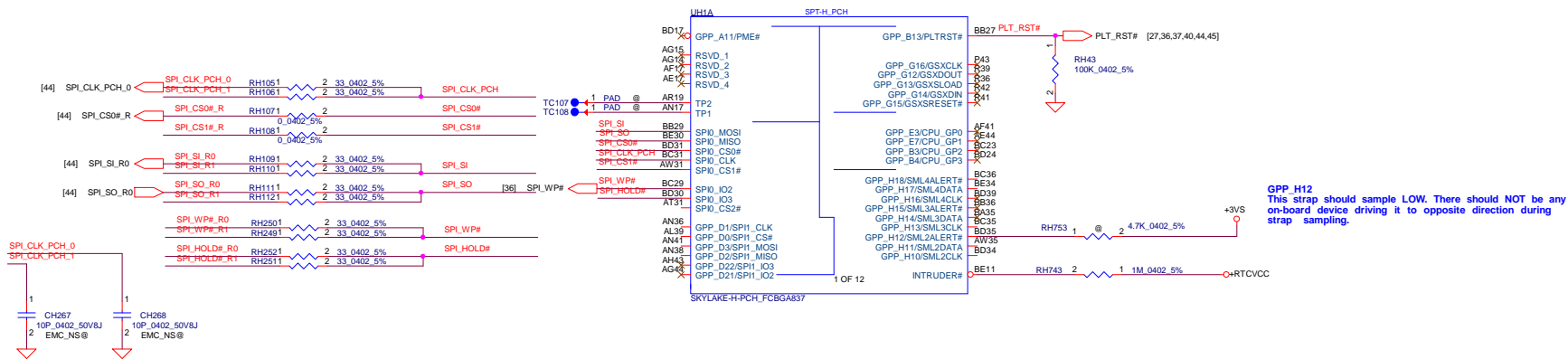






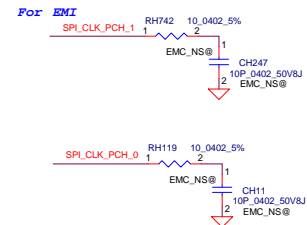
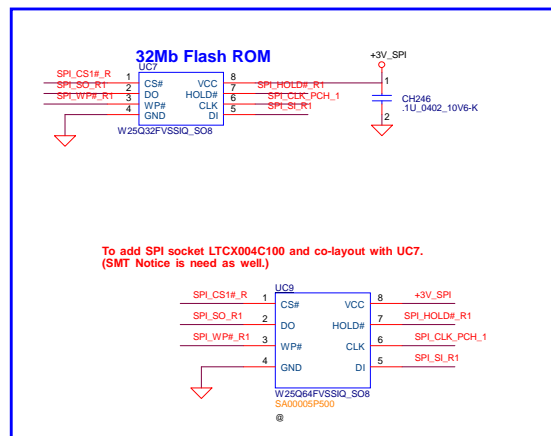
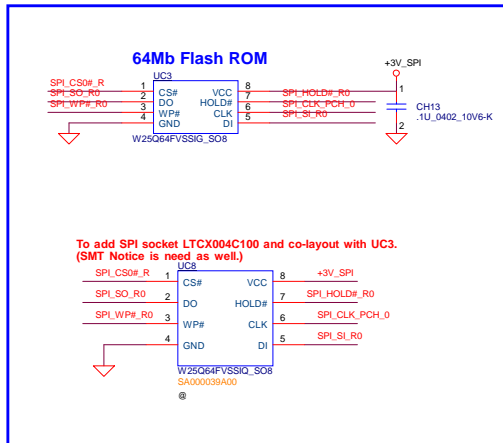


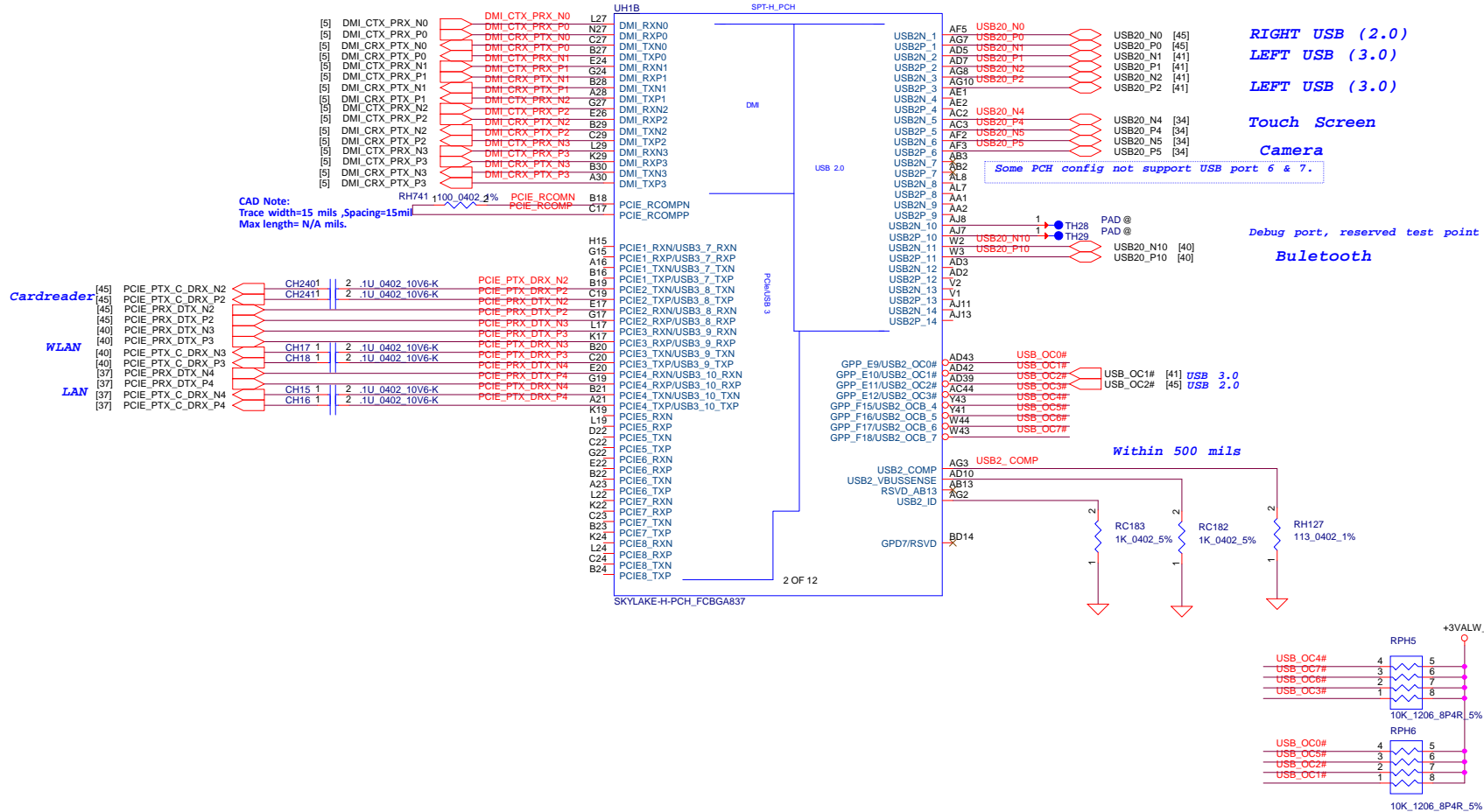


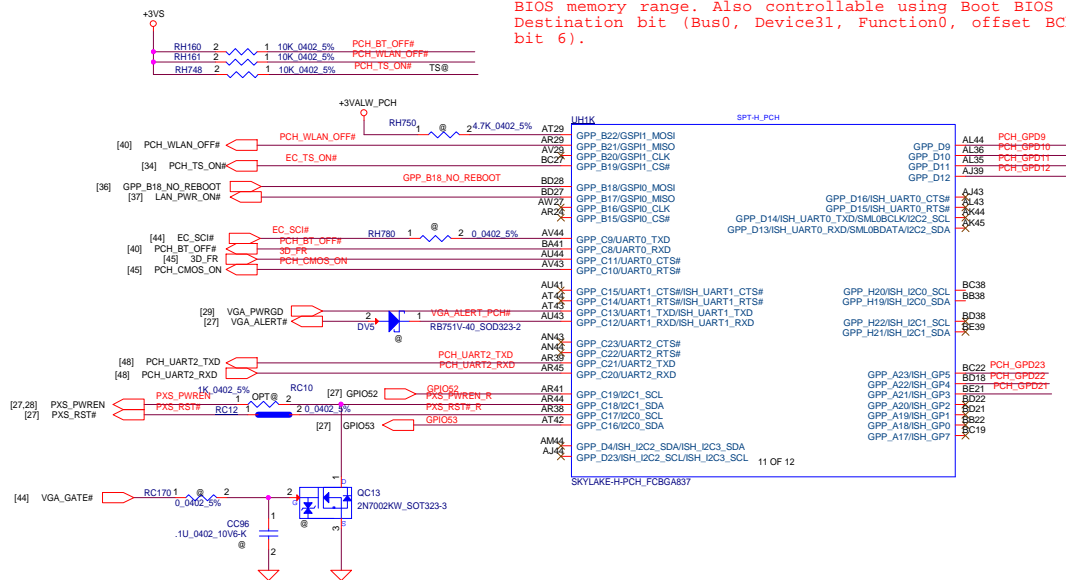


**SPI0\_MISO**  
 SPI0\_MISO  
 This signal has an internal pull-up.  
 This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

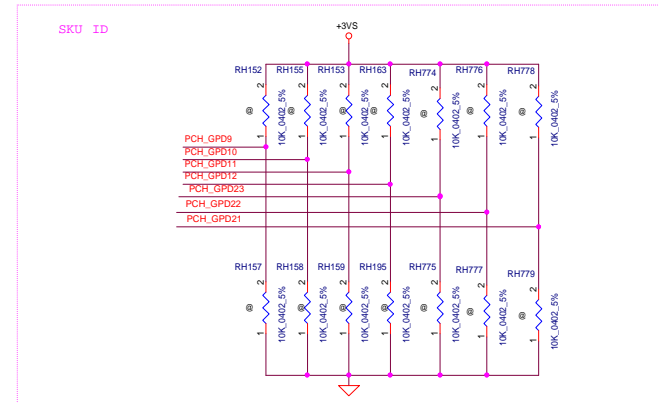
**+3V\_SPI**  
 1. If support DS3, connect to +3V/S and don't support EC mirror code;  
 2. If don't support DS3, connect to +3VALW\_PCH and support EC mirror code.



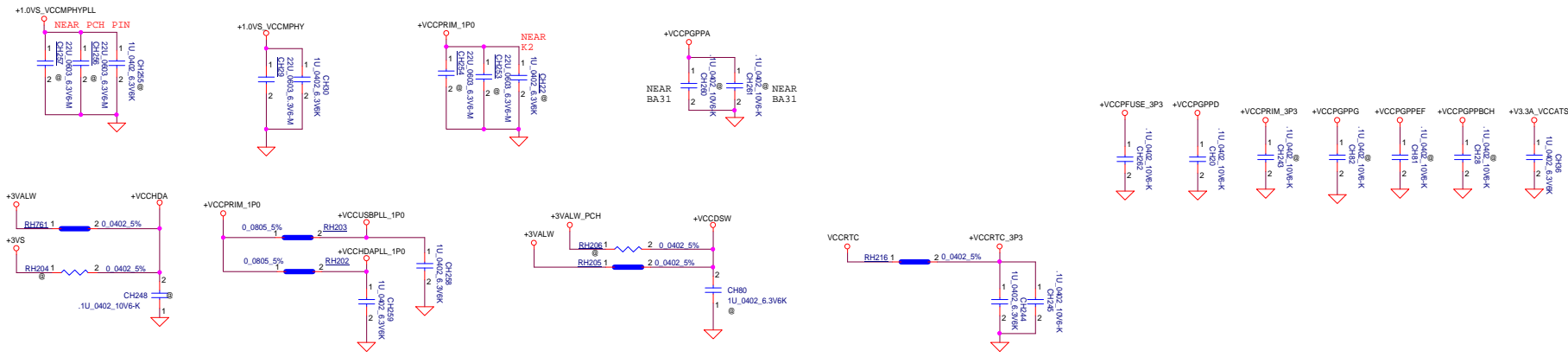
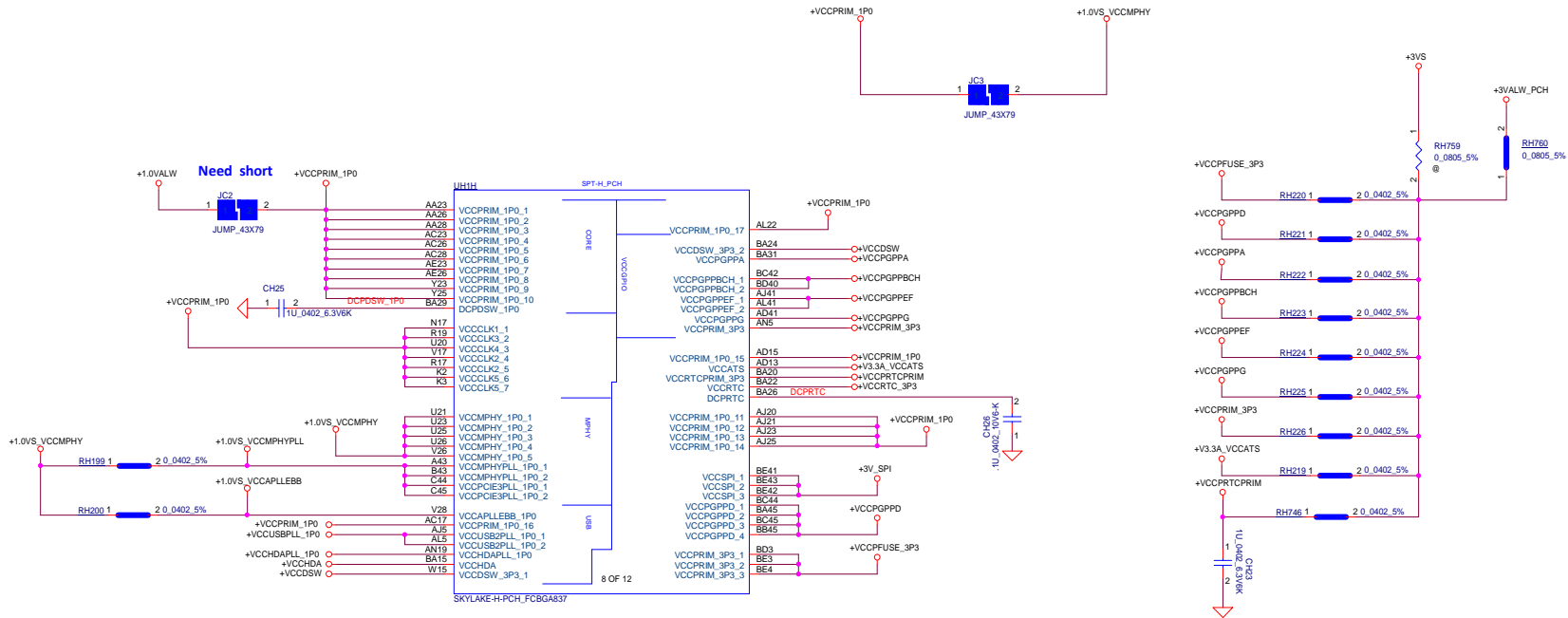


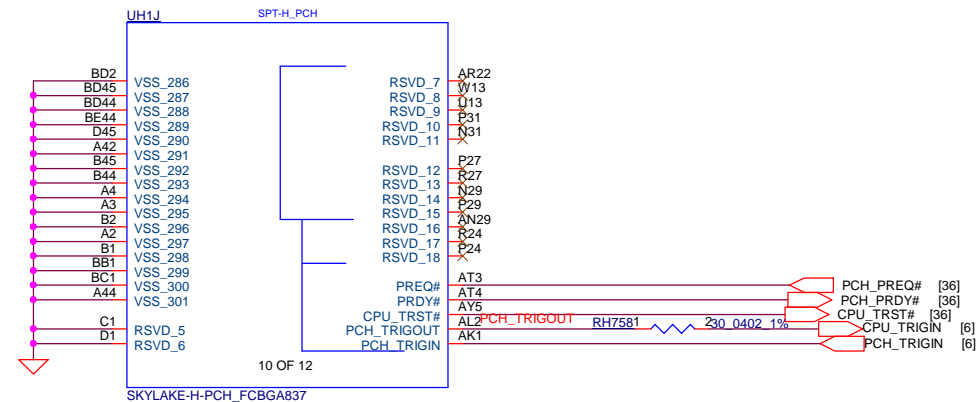
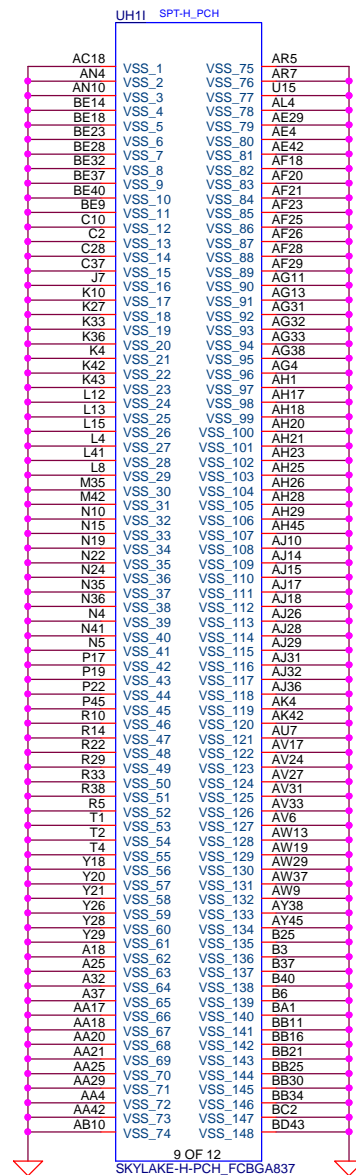
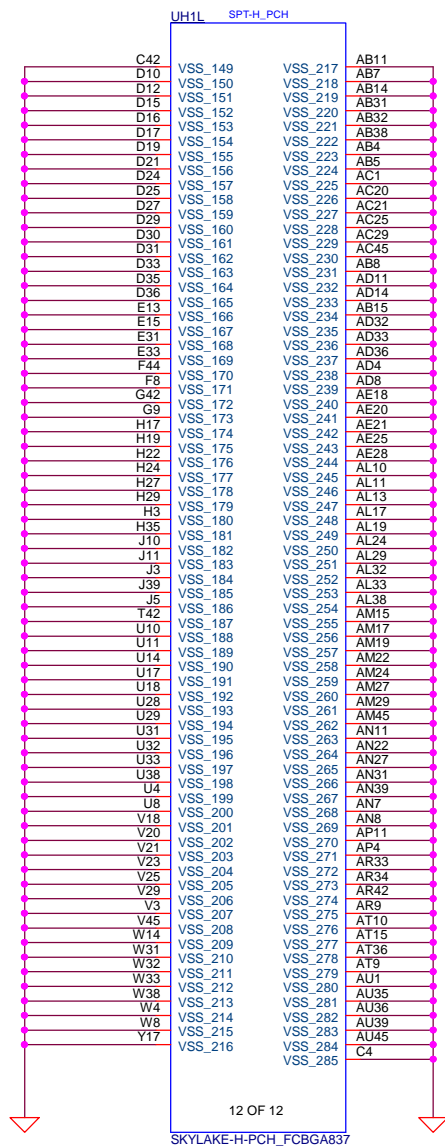



Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC



Function	PCH_GPD9	PCH_GPD10	PCH_GPD11	PCH_GPD12	PCH_GPD21	PCH_GPD22	PCH_GPD23
17"	0	X	X	X	X	X	X
15"	1	X	X	X	X	X	X
non 3D Camera	X	0	X	X	X	X	X
3D Camera	X	1	X	X	X	X	X
non-touch	X	X	0	X	X	X	X
touch	X	X	1	X	X	X	X
SDV	X	X	X	X	0	0	0
SIV	X	X	X	X	0	0	1
SIT	X	X	X	X	0	1	0
SVT	X	X	X	X	0	1	1



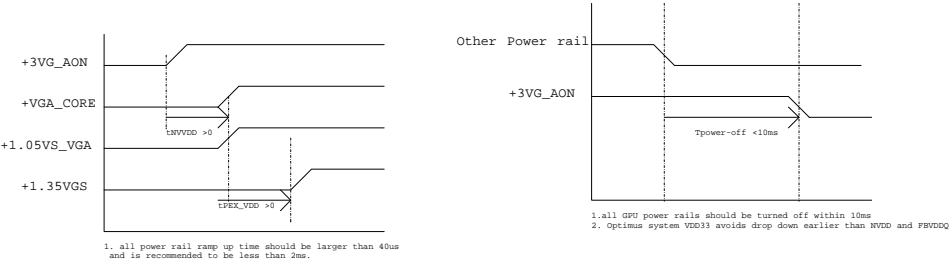


Security Classification		LC Future Center Secret Data		<b>Title</b>  <b>PCH (9/9) VSS</b> 	
Issued Date	2015/02/26	Deciphered Date	2016/02/26		
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N16P-GX GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	IN	-	System side PCIe reset Monitor
GPIO9	I/O	-	VGA_ALERT#
GPIO10	OUT	-	Memory VREF Control (100K pull Down)
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN	-	AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16	IN	N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT	-	GPU PCIe self-reset control
OVERT	I/O	-	Active Low Thermal Catastrophic Over Temperature

N16P-GX Power Sequence



Performance Mode P0 TDP at Tj = 102 C\* (DDR5)

Products	GPU (4)	Mem (1.5)	NVCLK MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)				I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(A)	(W)			(A)	(W)	(A)	(W)
N16P-GX 128bit 2GB DDR5	50	3.27	2505	TBD	51.1	TBD	3.46	4.67	8.75	11.81	TBD	TBD			2.57	2.7	0.34	TBD

N16P-GX Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

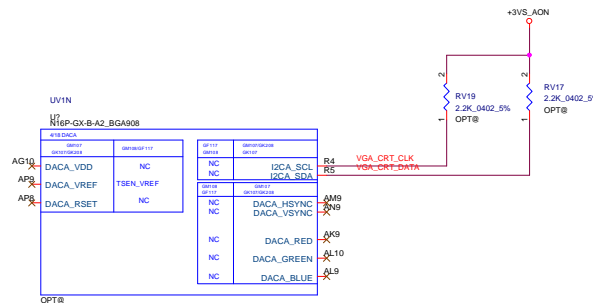
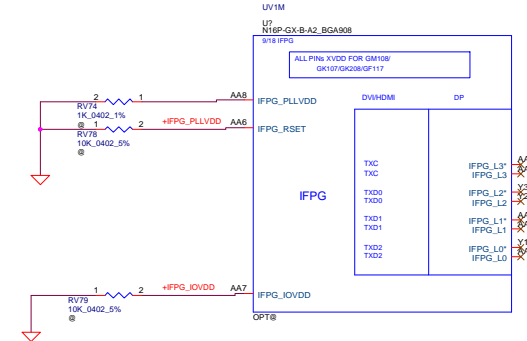
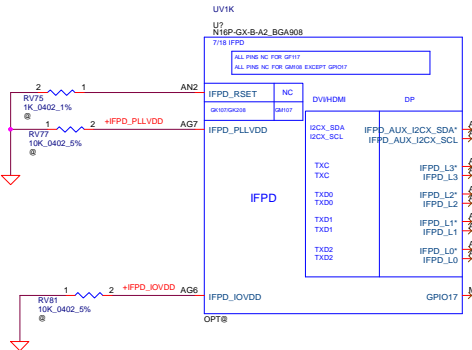
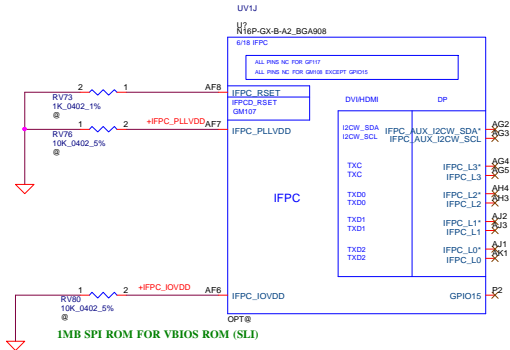
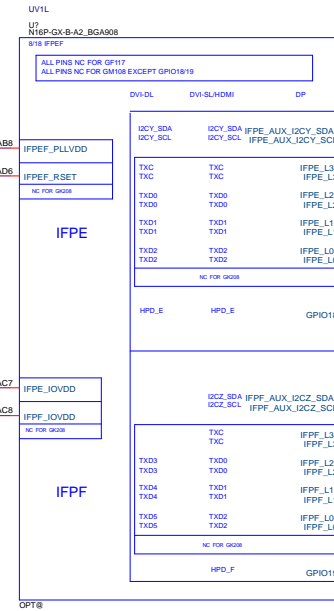
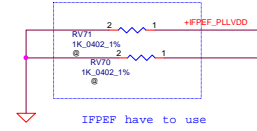
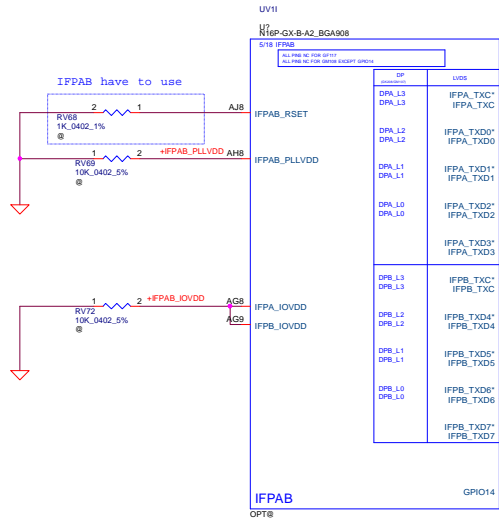
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

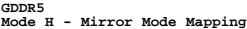
N16P-GX Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED



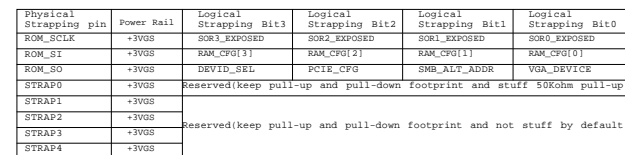






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Title		N16P-GX_VRAM I/F			
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Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

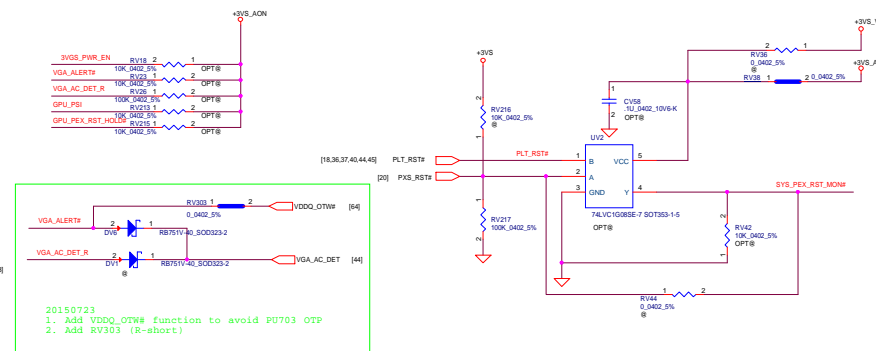
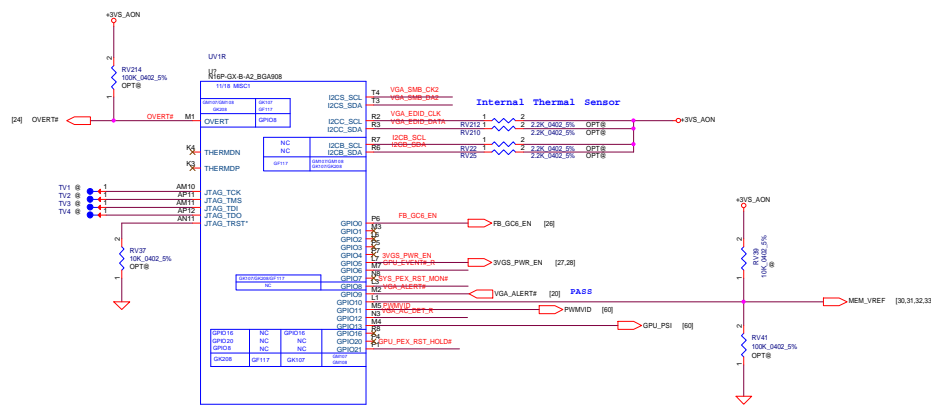
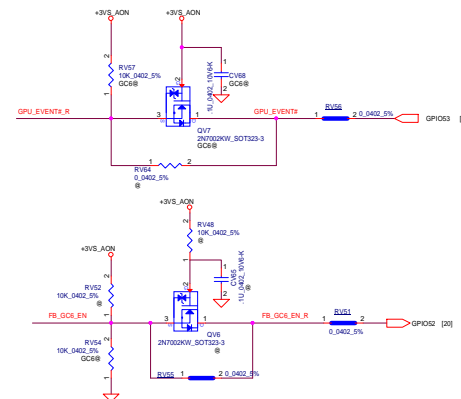
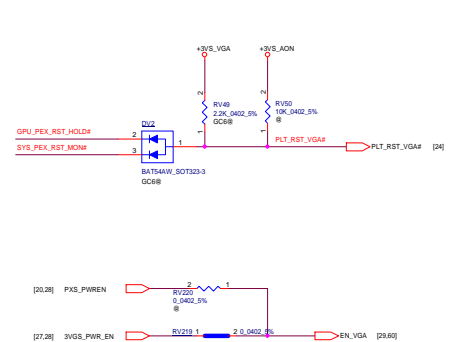
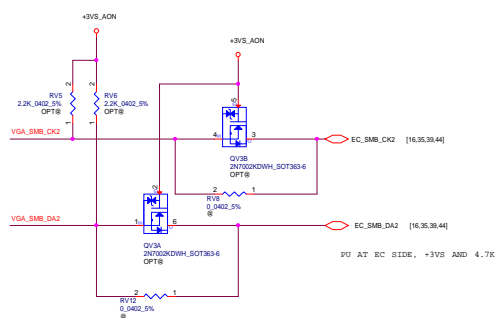
DEVID_SEL	
0	(Default)
1	


PCIE_CFG	
0	(Default)
1	

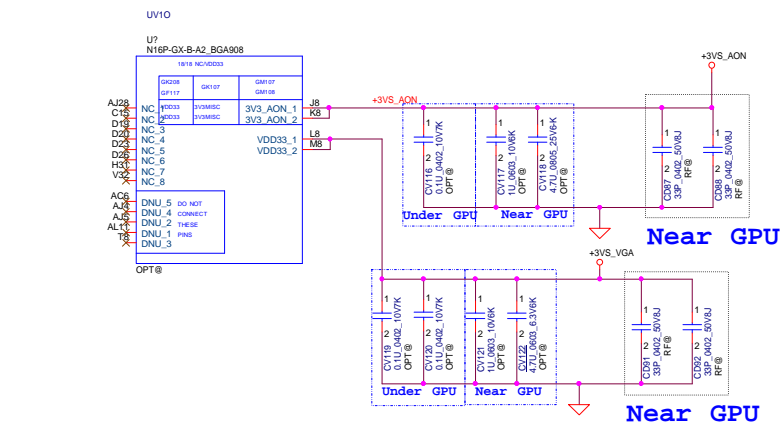
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 30)
1	VGA Device (Default)

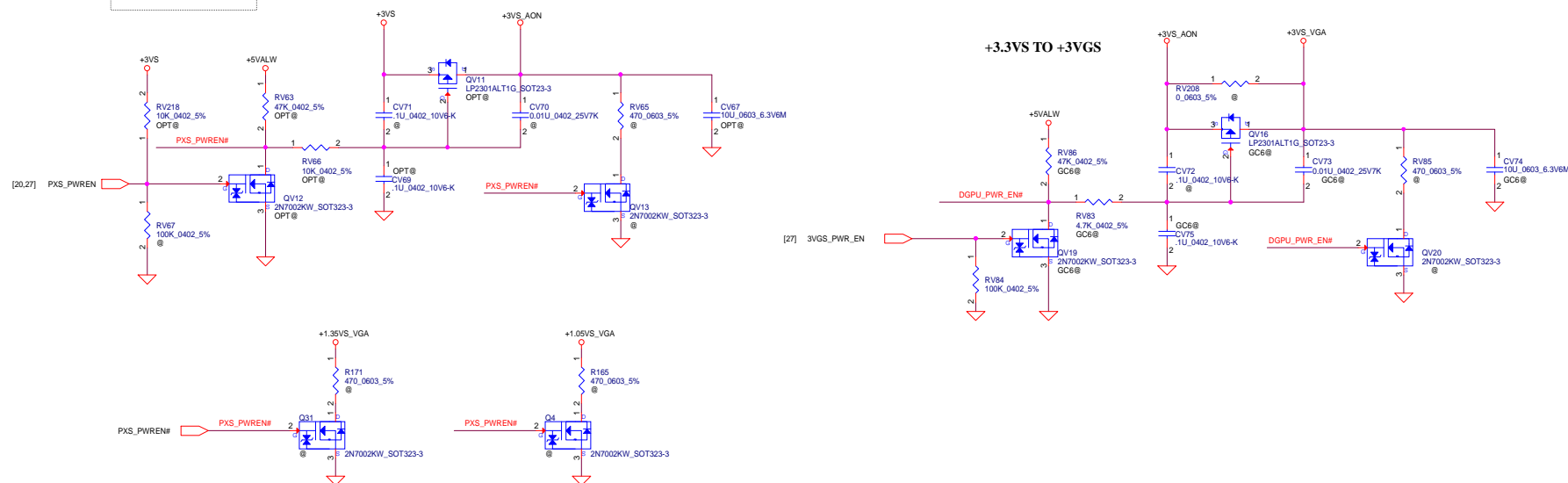
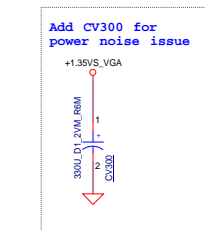
GPU	FB Memory (GDDR5)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16P-GX	Samsung	K4G20 325FD-FC03 128X16	PD 5K	PD 5K	PD 5K	PU 50K	NC	NC	NC
		K4G41 325FD-HC03 256X16	PD 20K						
	Hynix	H5GC2H24BFR-T2C 128X16	PD 10K						
		H5GC4H24AJR-T2C 256X16	PD 34.8K						
	Micron	EDW20 32HBBG-6A-F 128X16	PD 30.1K						
		EDW40 32HABG-60-F 256X16	PD 24.9K						

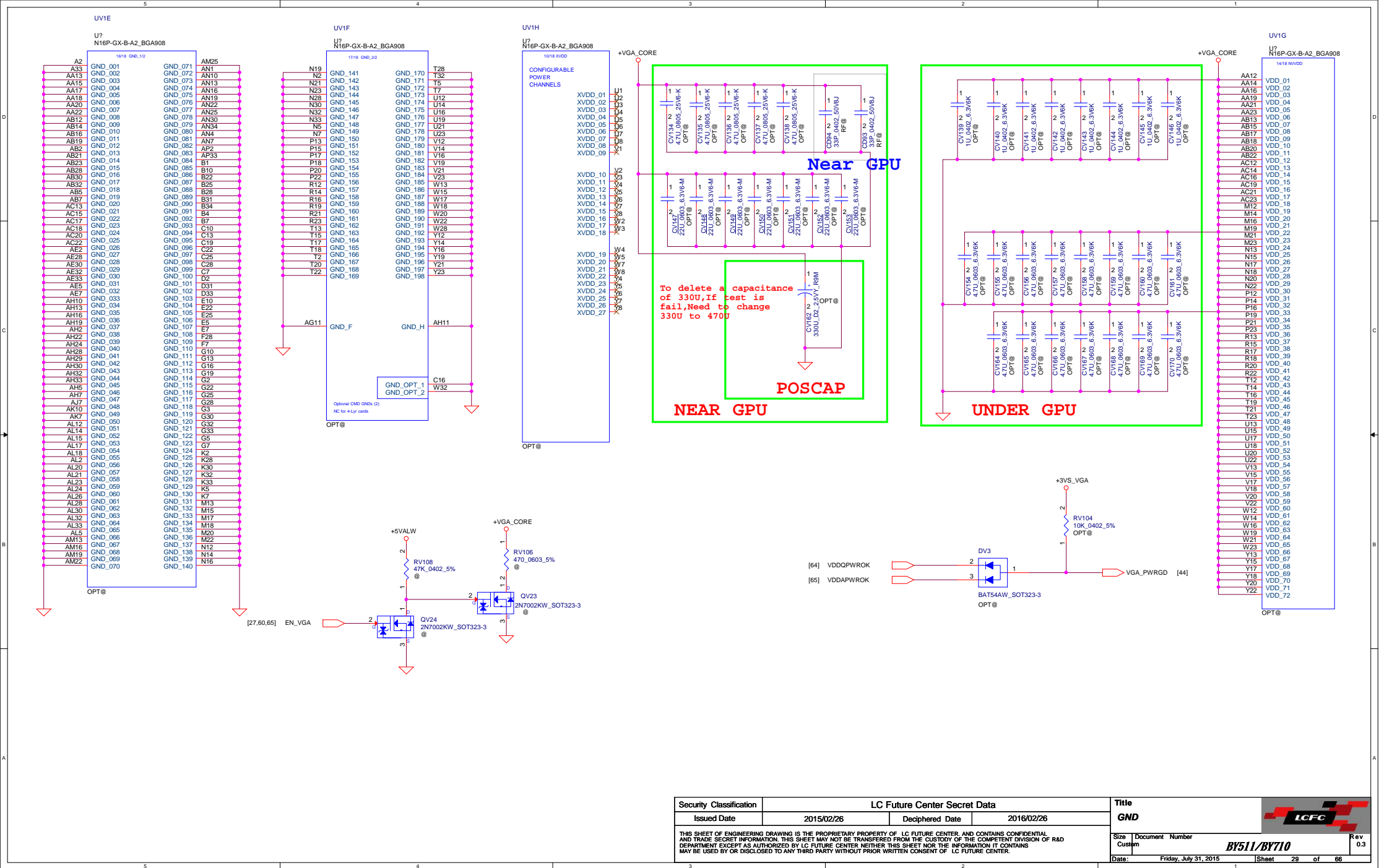



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		B7511/2710		Friday, May 31, 2015		
				Sheet		27 of 66



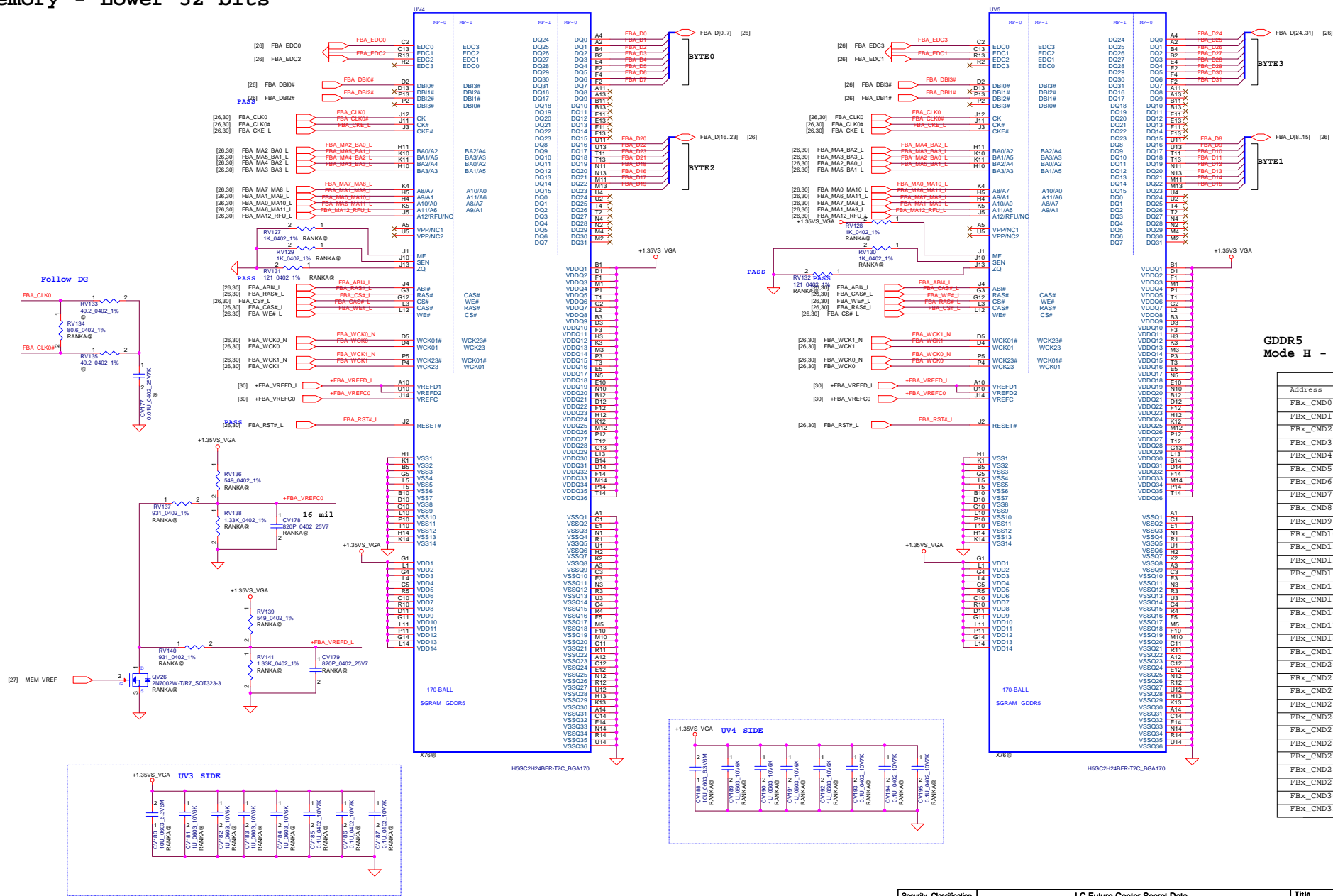
CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2ohm
FB_CAL_x_PU_GND	40.2ohm
FB_CAL_xTERM_GND	60.4ohm





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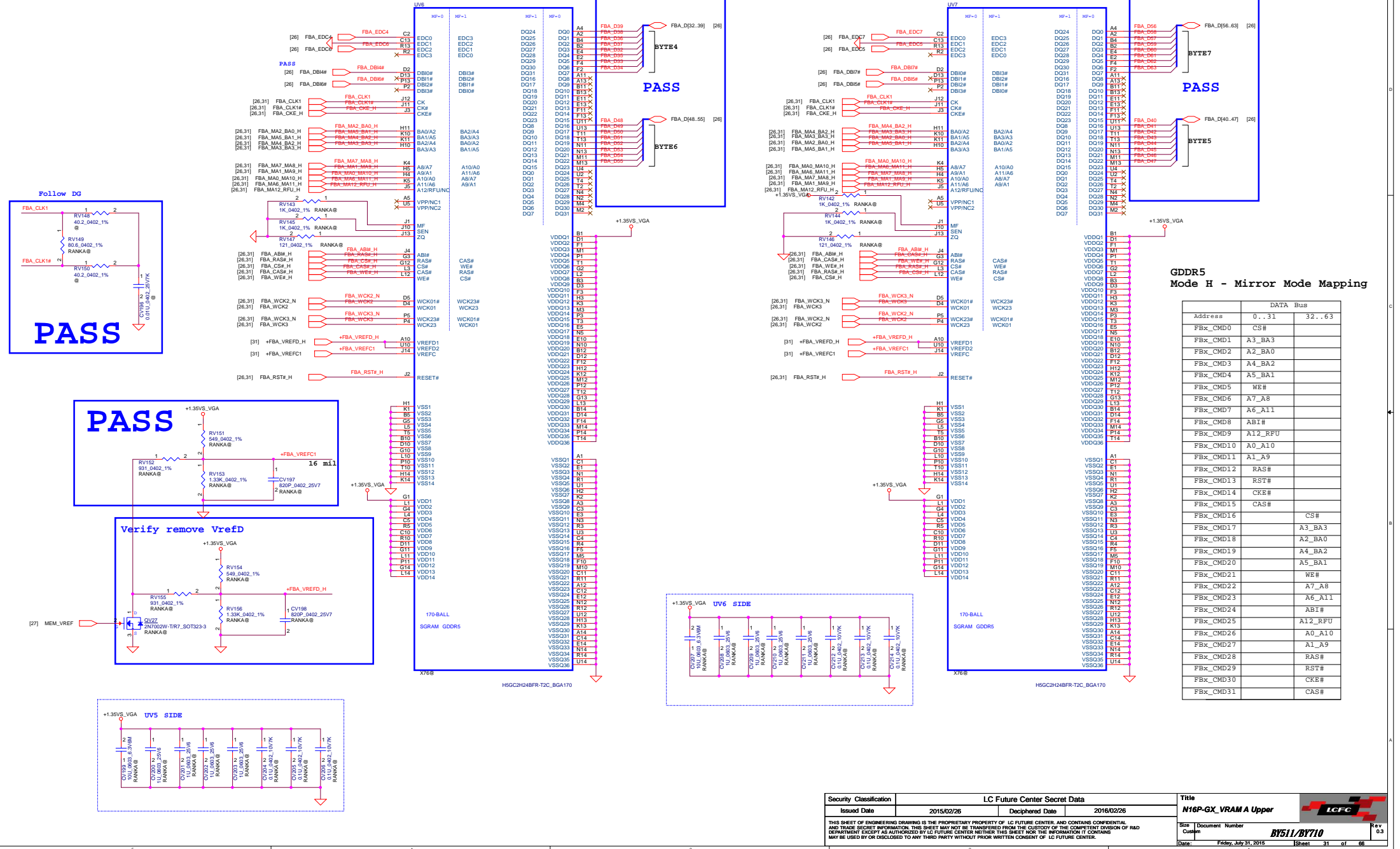
**Memory - Lower 32 bits**



GDDR5  
Mode H - Mirror Mode Mapping

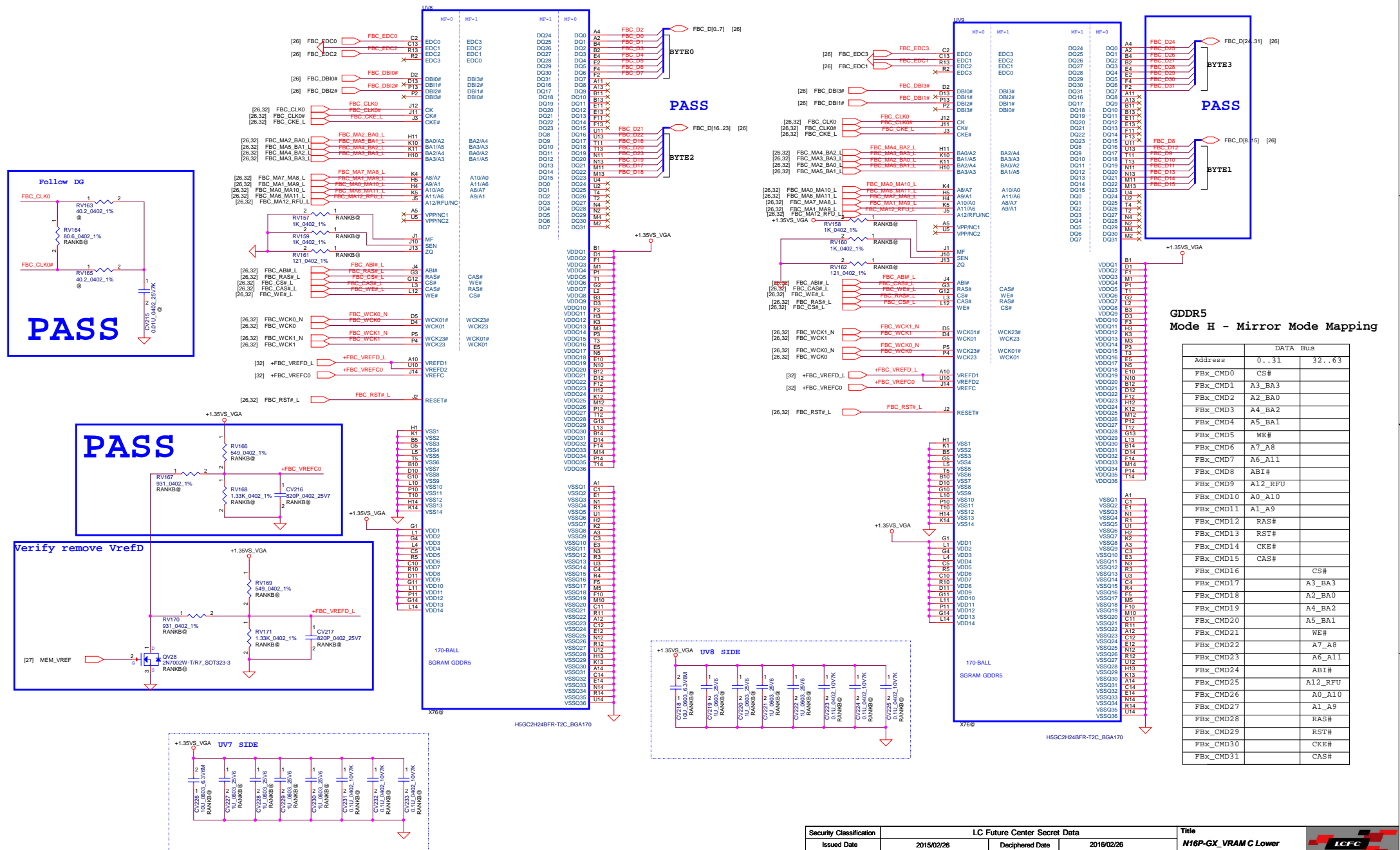
	DATA Bus	
Address	0...31	32...63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	AB1#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		AB1#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Memory - Upper 32 bits



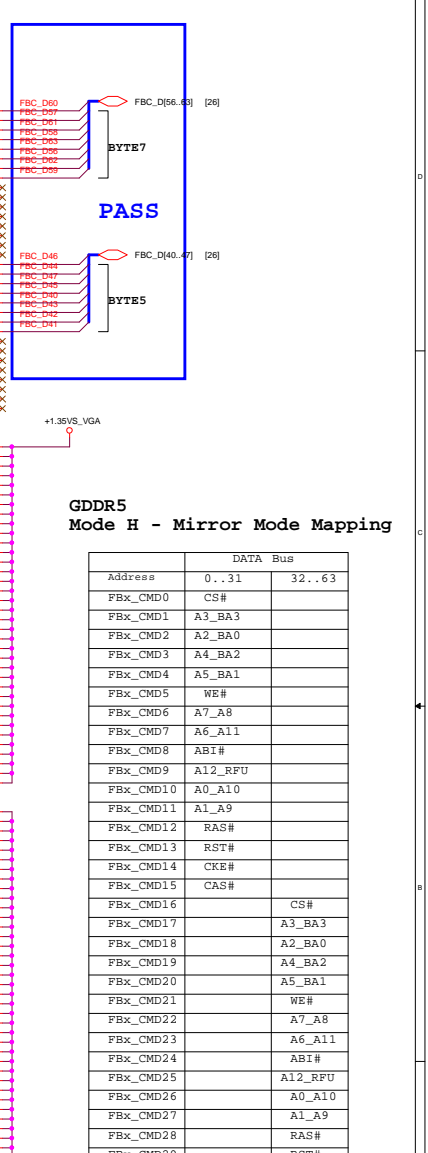
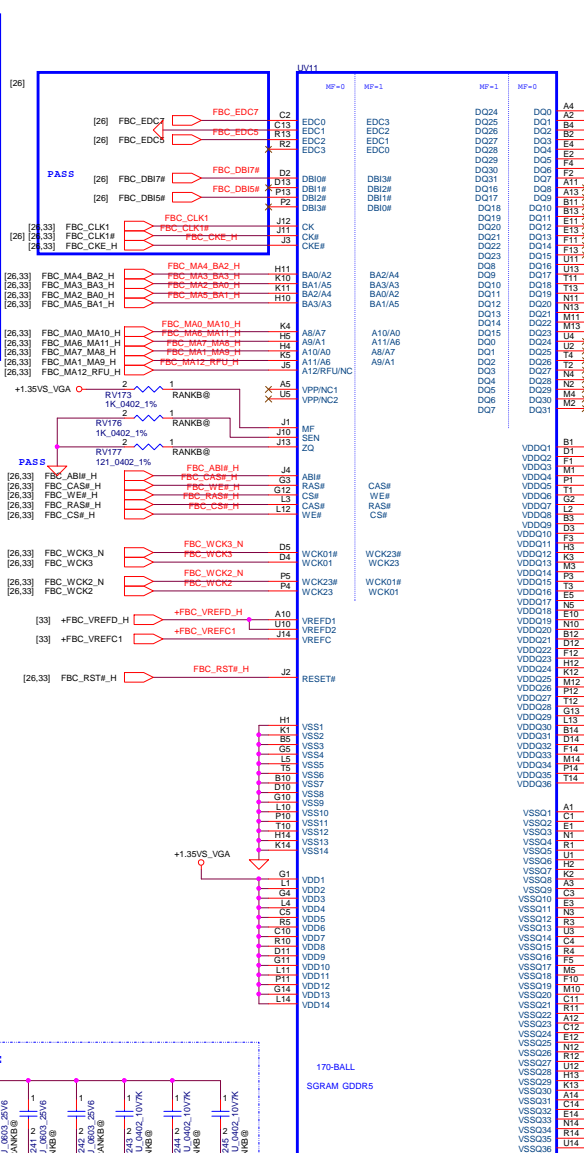
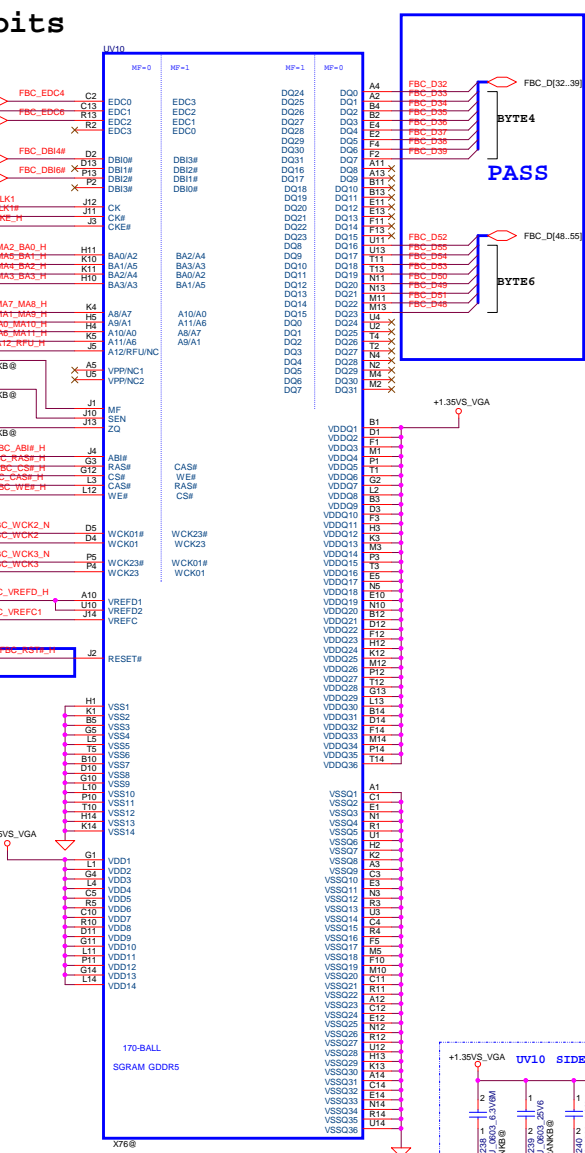
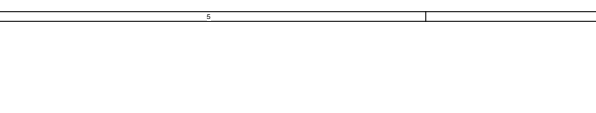
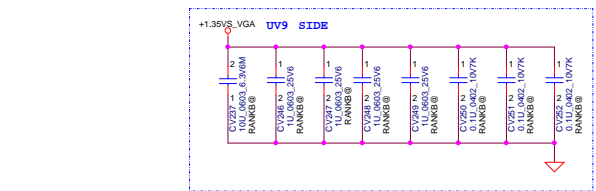
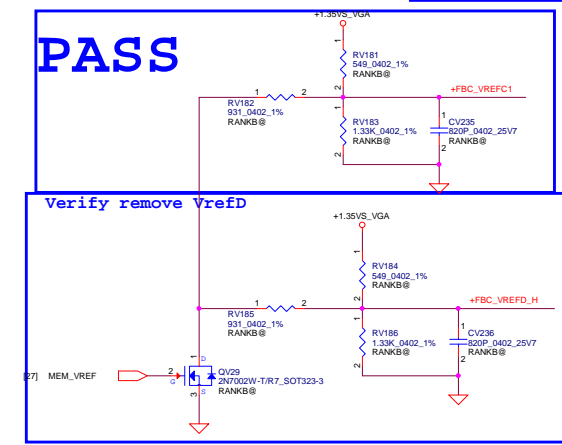
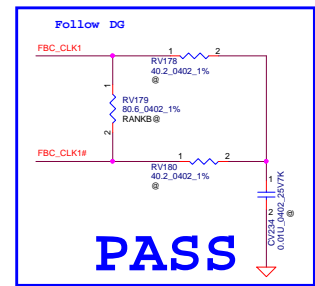


# Memory Partition C - Lower 32 bits





Memory Partition C - Upper 32 bits



GD55 Mode H - Mirror Mode Mapping

Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA2	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	AB1#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA2
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		AB1#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#



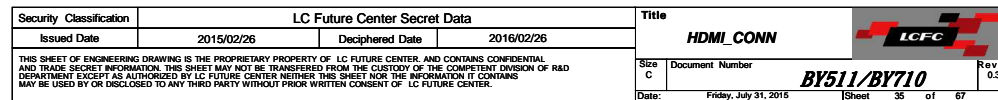




TABLE : CPU ITP DEBUG REPORT

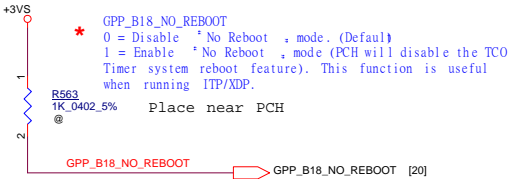
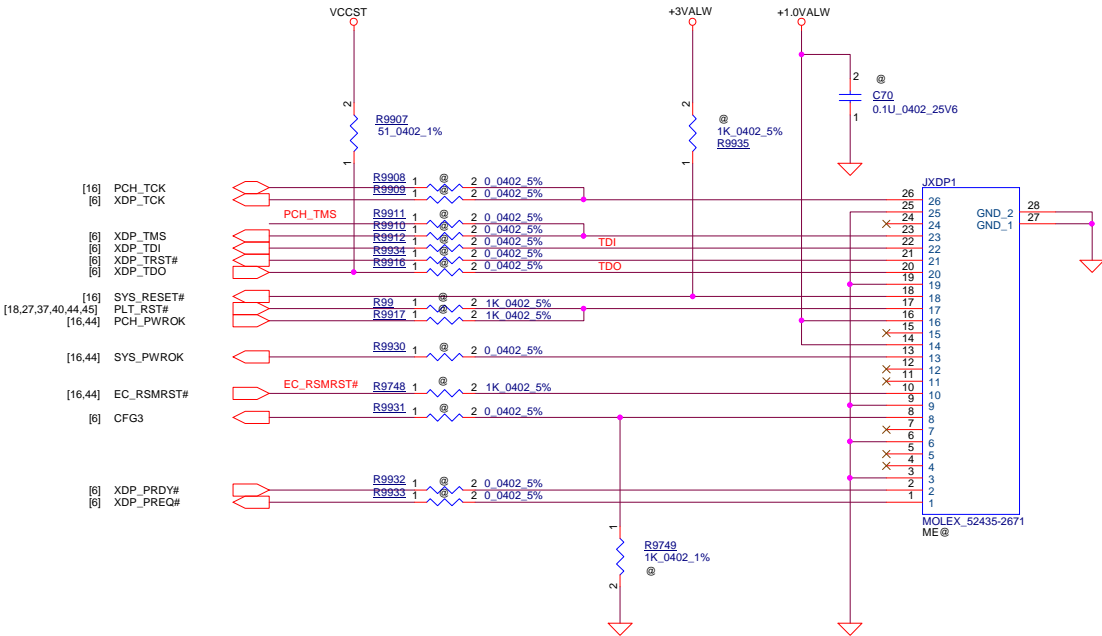
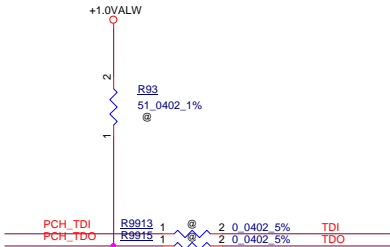
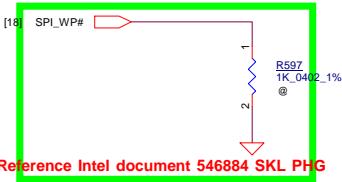
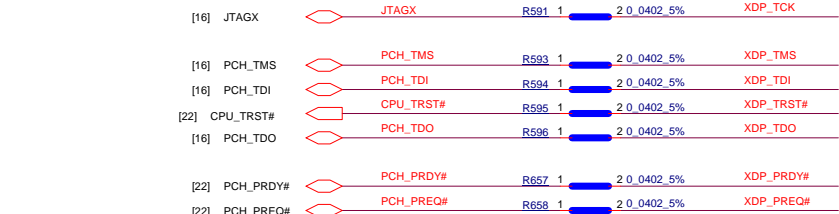
	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

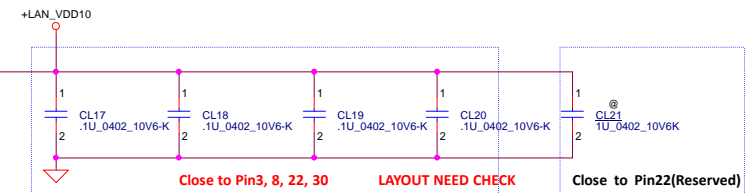
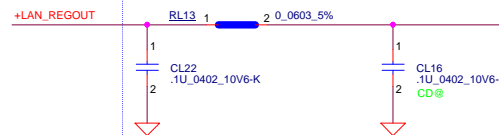
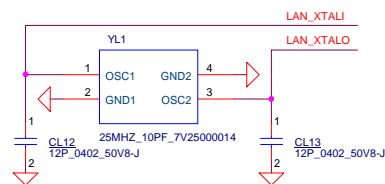
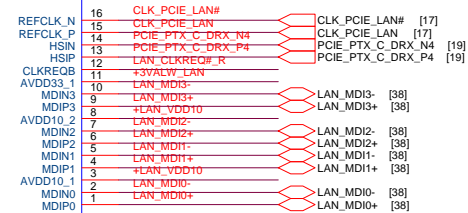
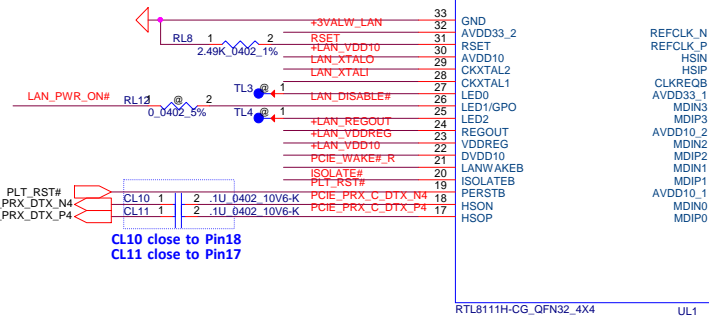
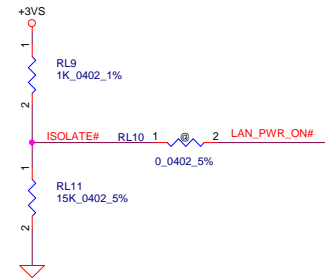
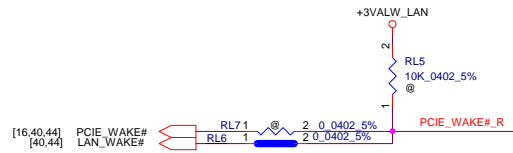
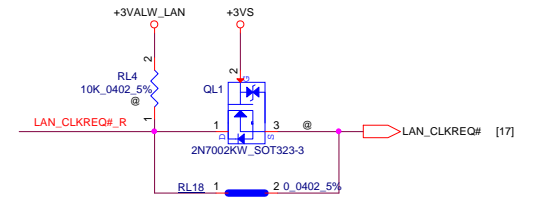
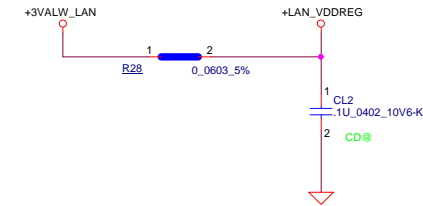
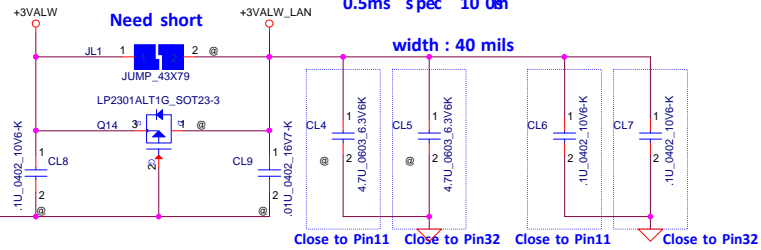
TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default )	NO ASM

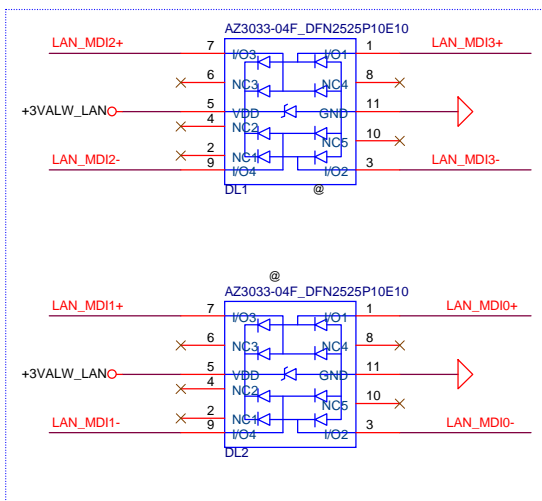




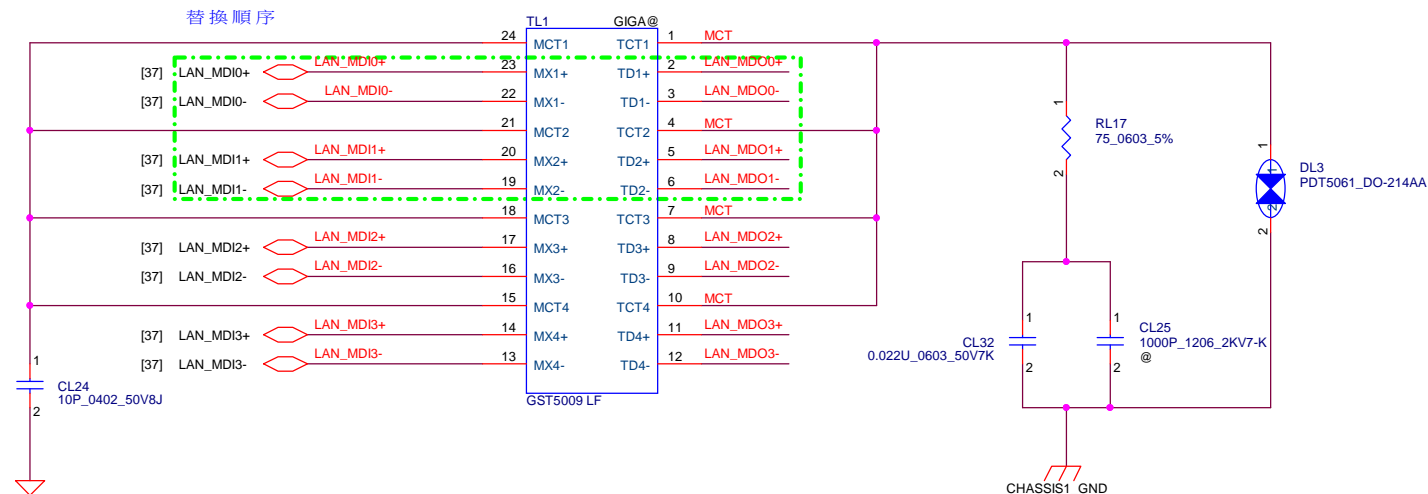
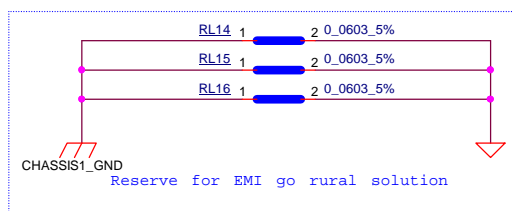
Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1  
+LAN\_REGOUT: Width =60mil

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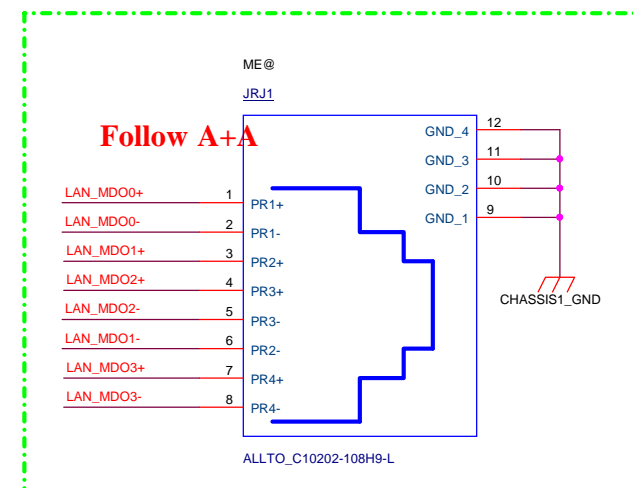
DL1/DL2  
1'S PN:SC300003M00




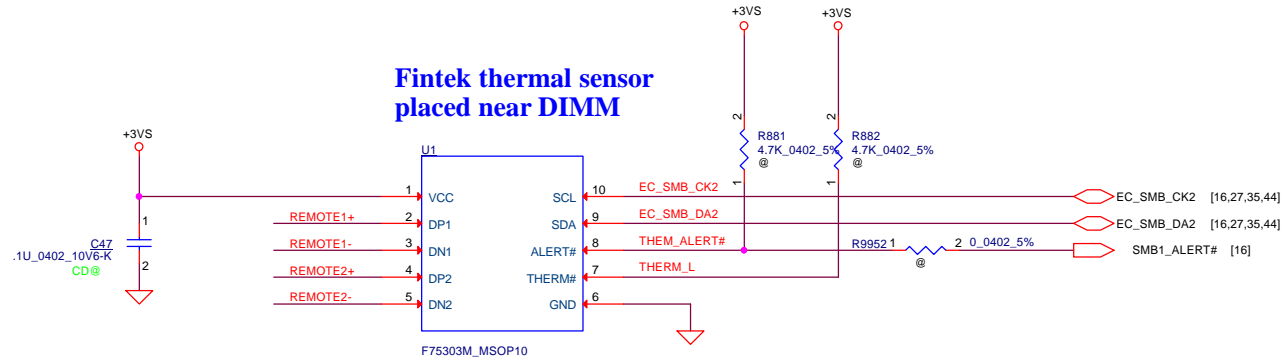
Place Close to TL1



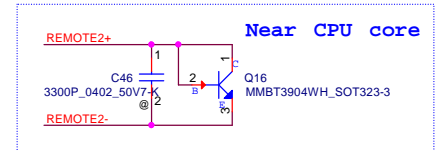
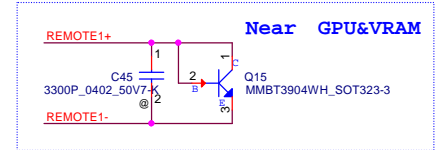
櫃 JRJ 1 CONN



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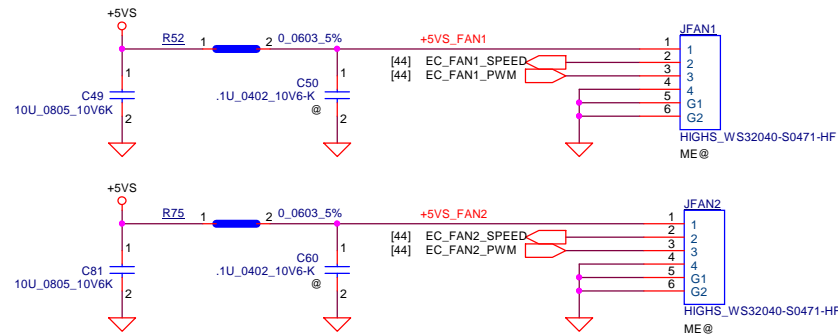



REMOTE+/-\_R, REMOTE1+/-, REMOTE2+/-:  
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## FAN Conn

Address 1001\_101xb



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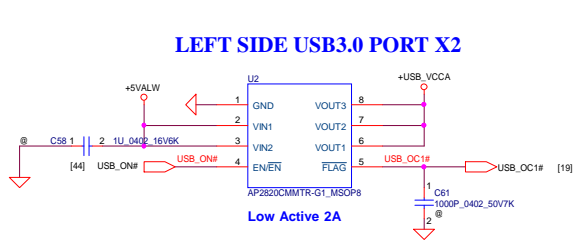


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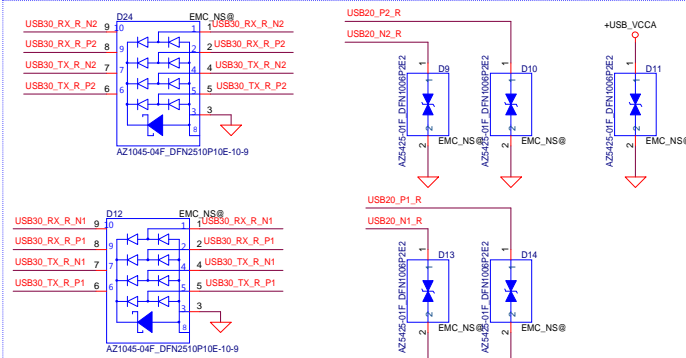
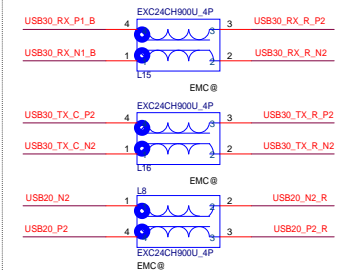
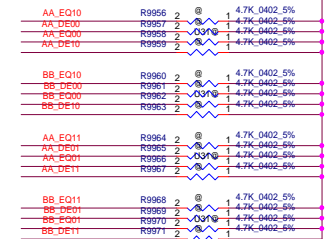
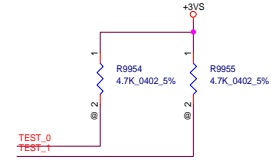
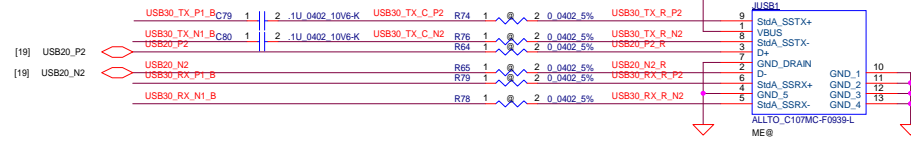




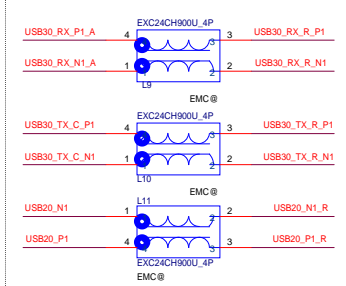
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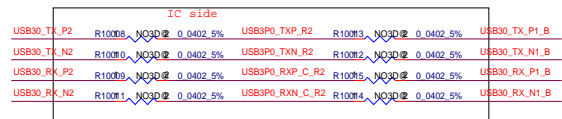
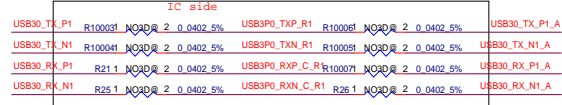
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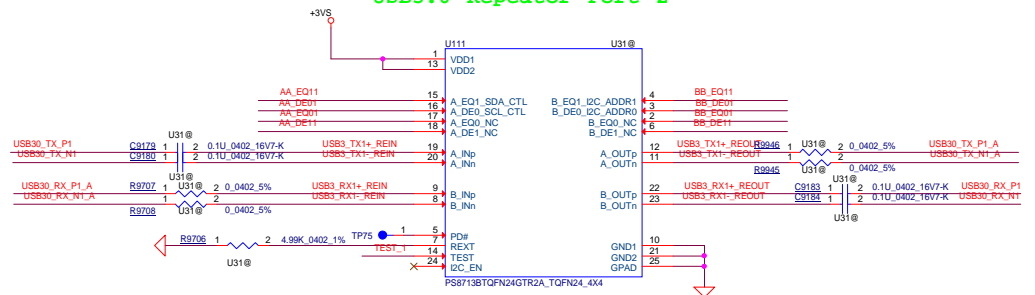
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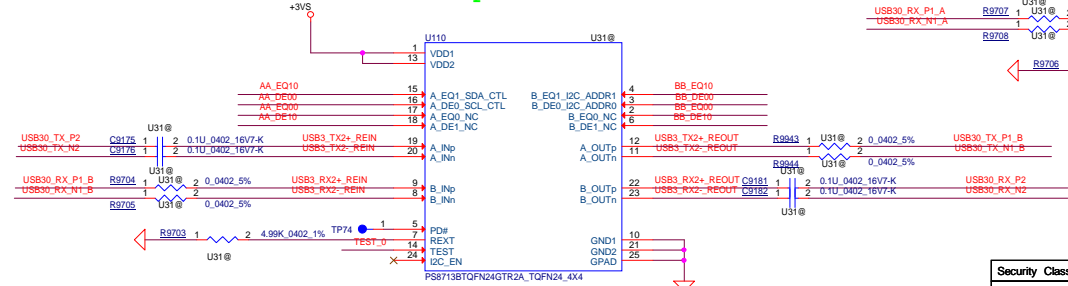
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## USB3.0 Repeater Port 2

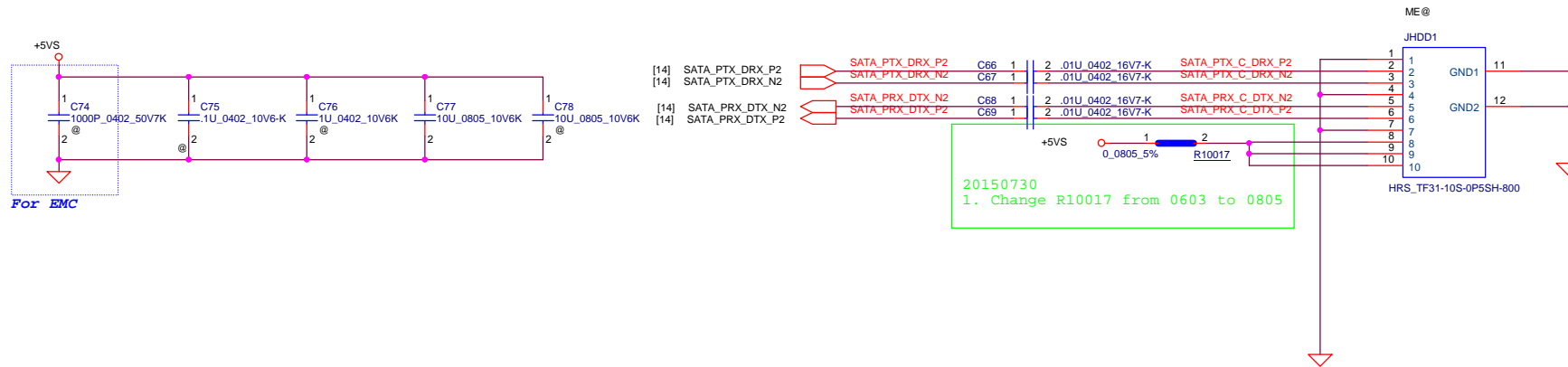


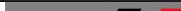
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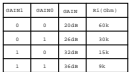
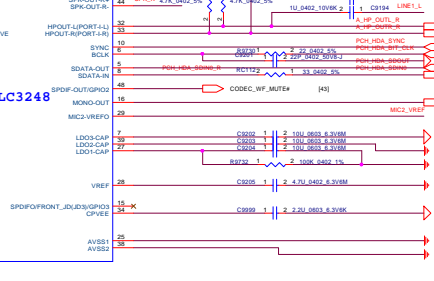
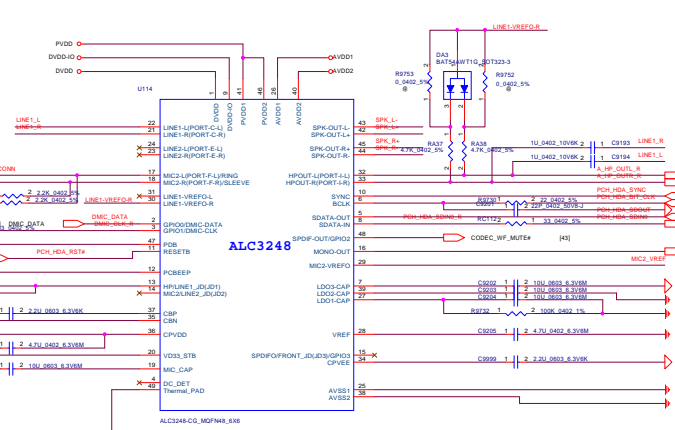
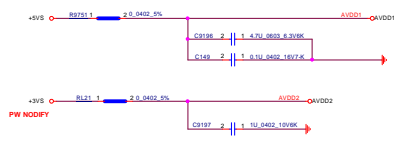


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# SATA HDD Conn.



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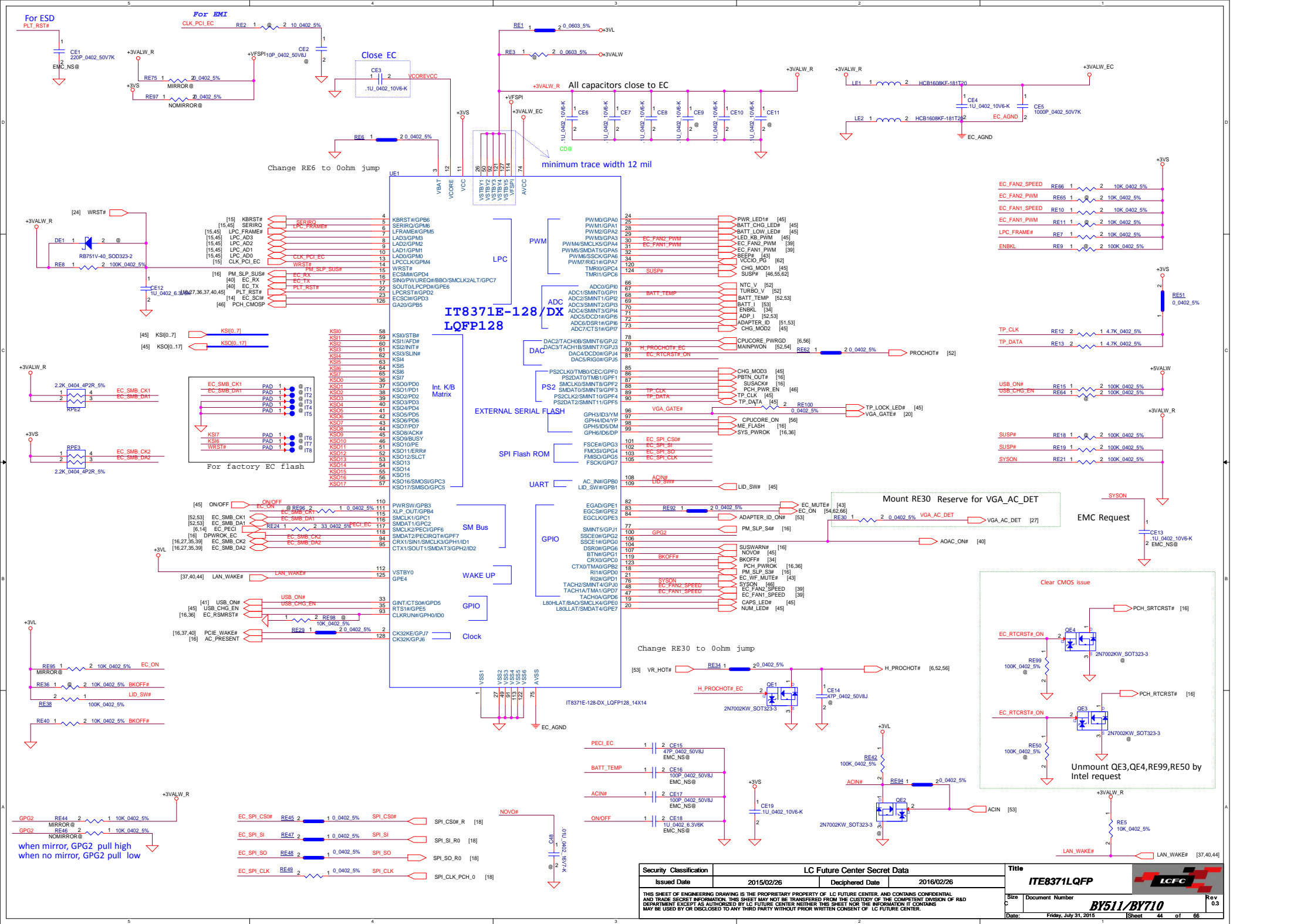


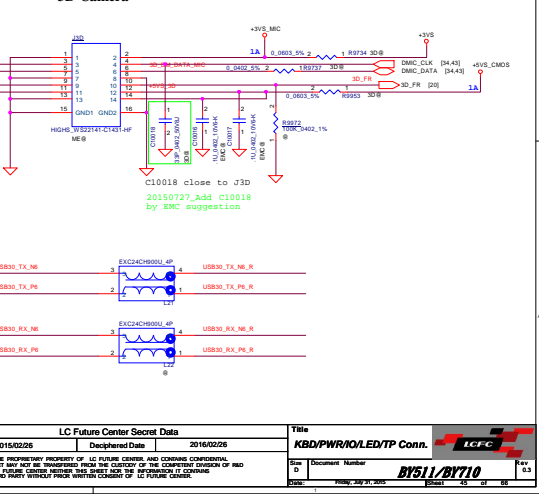
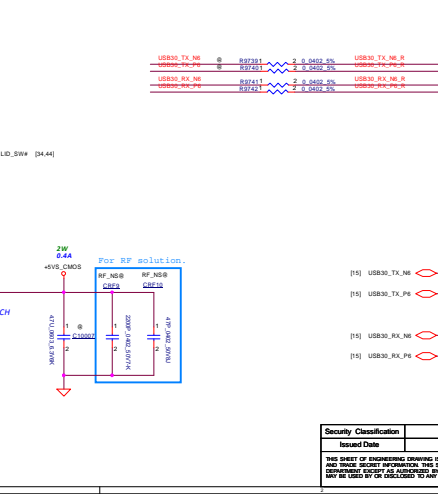
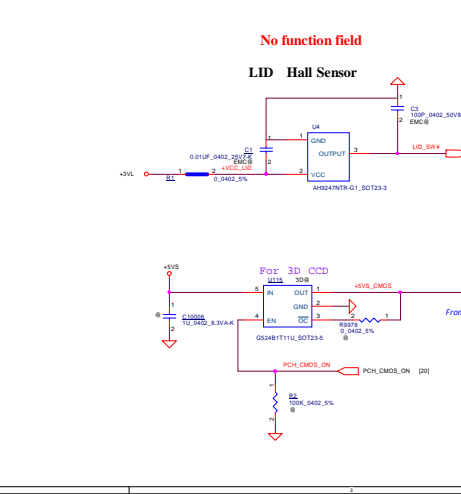
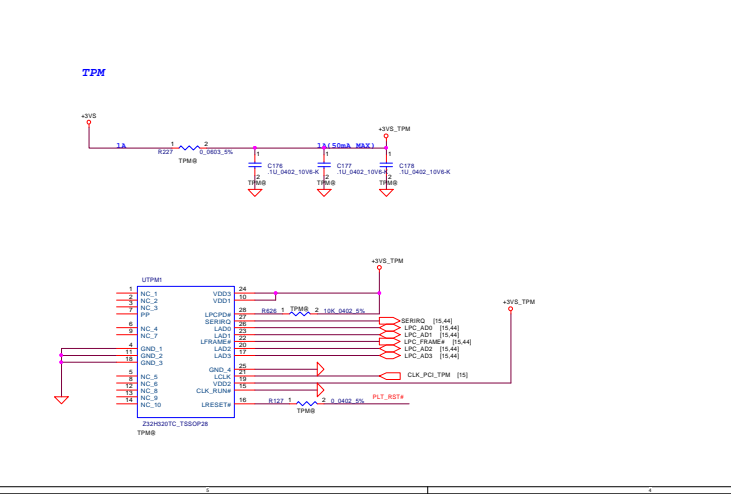
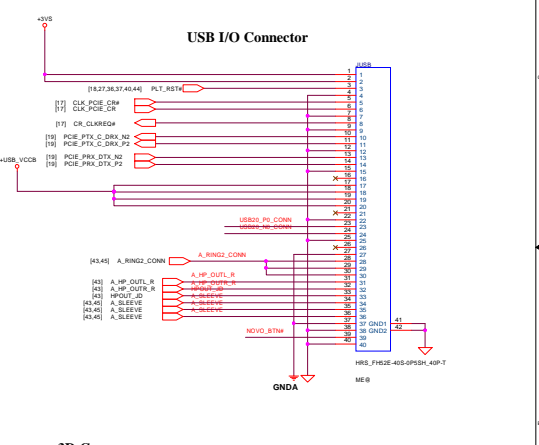
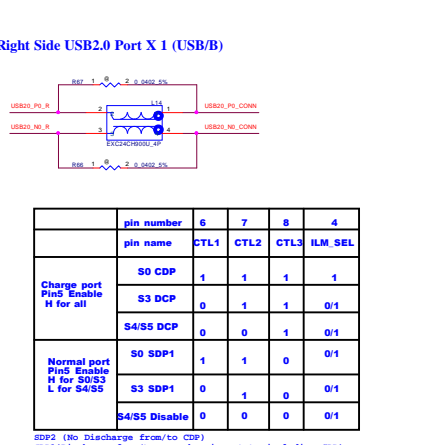
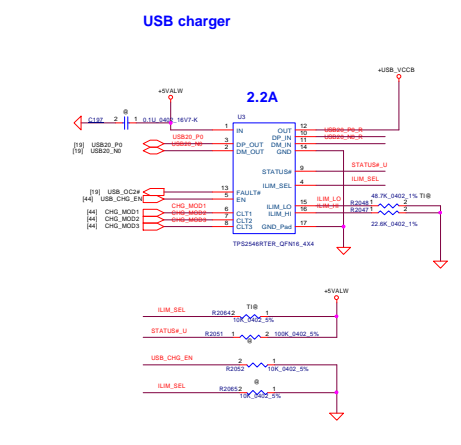
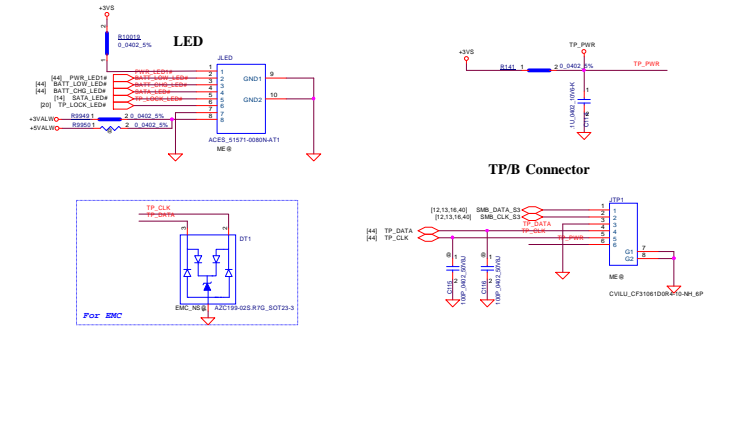
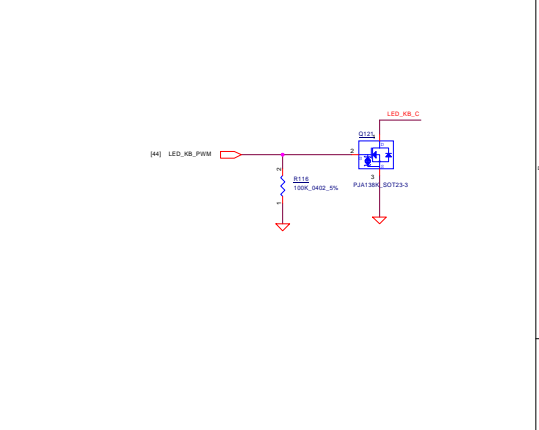
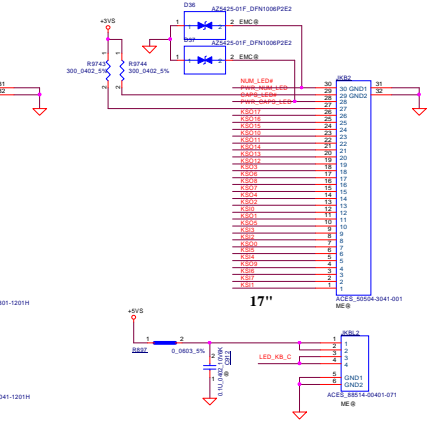
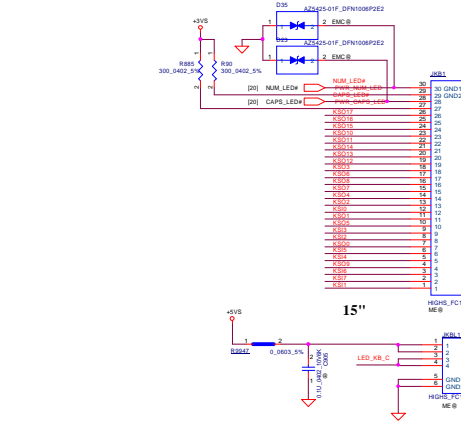
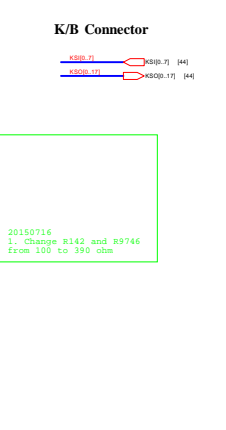
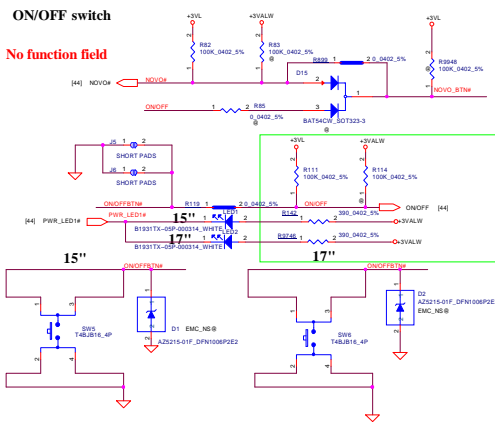
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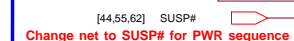
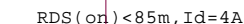
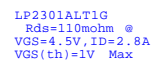
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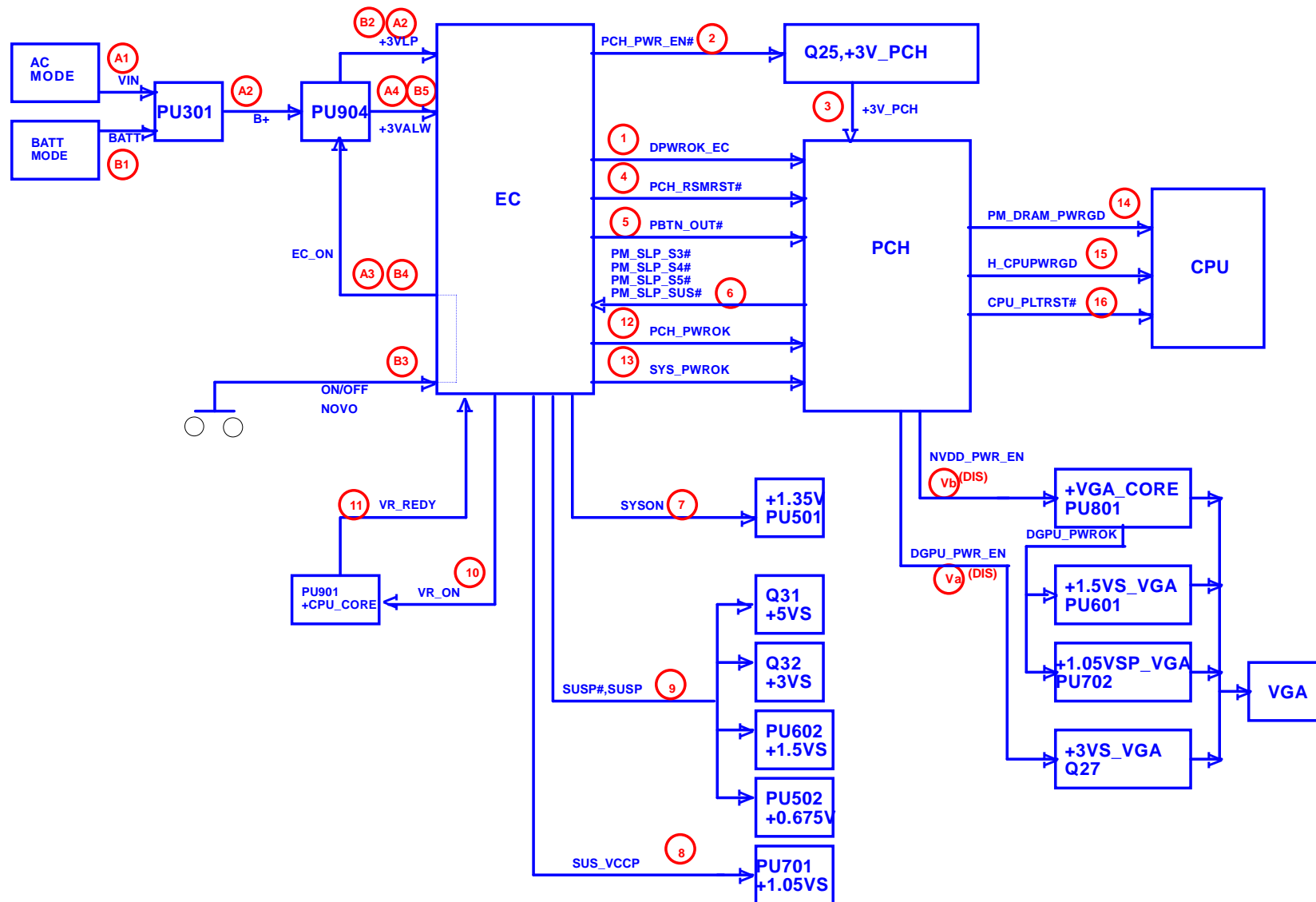




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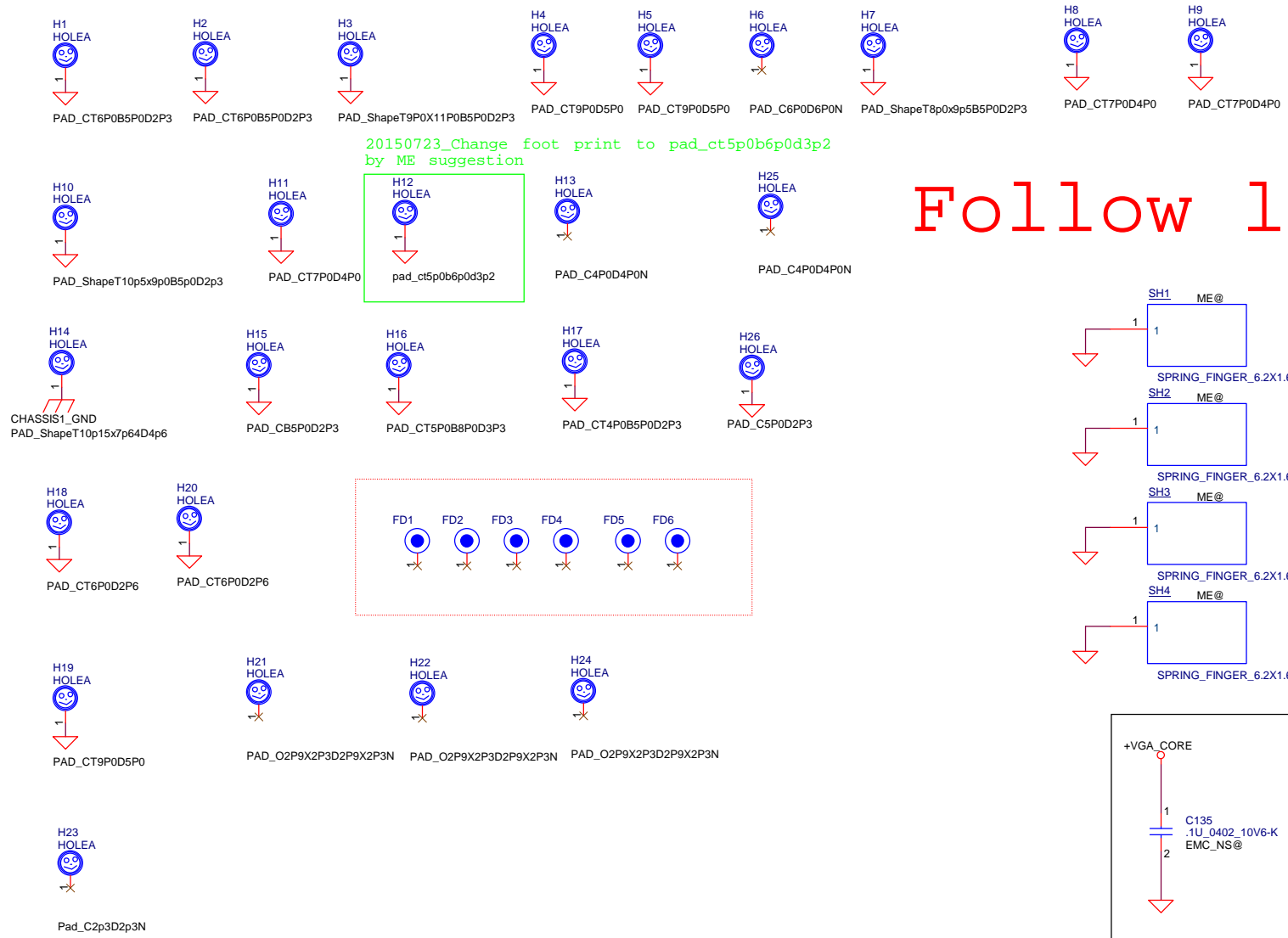
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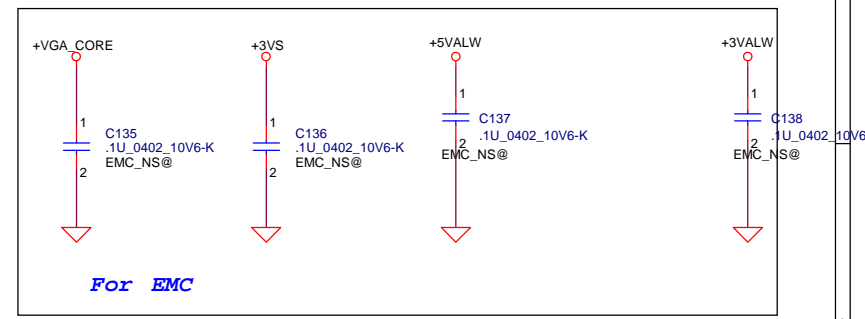
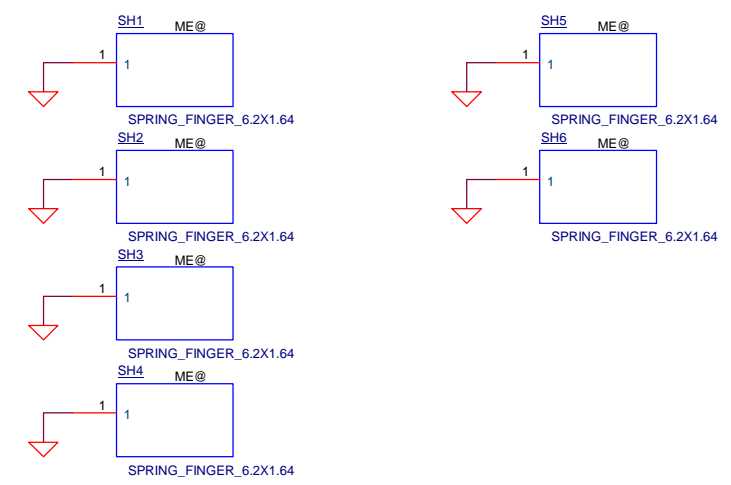
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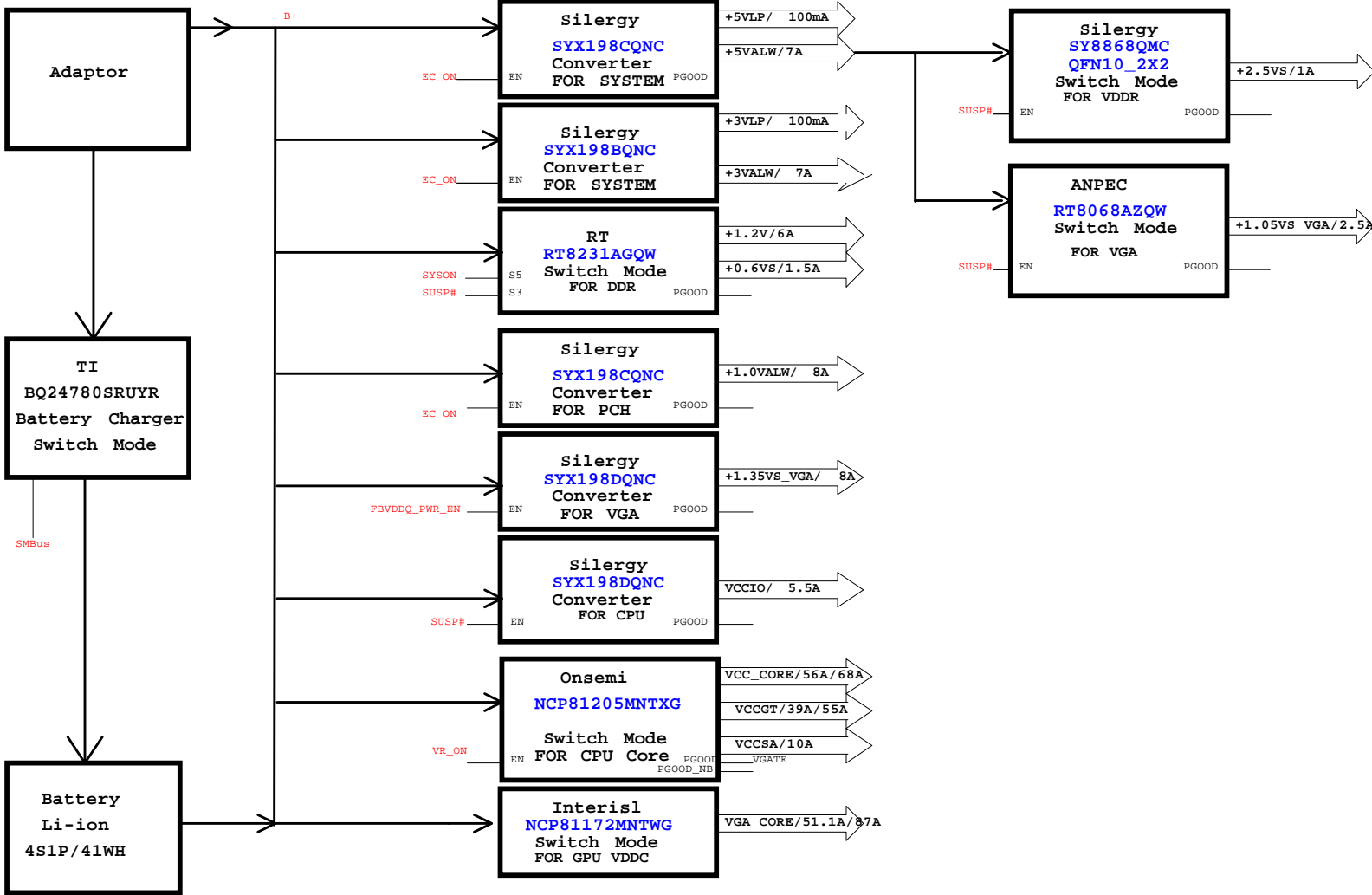
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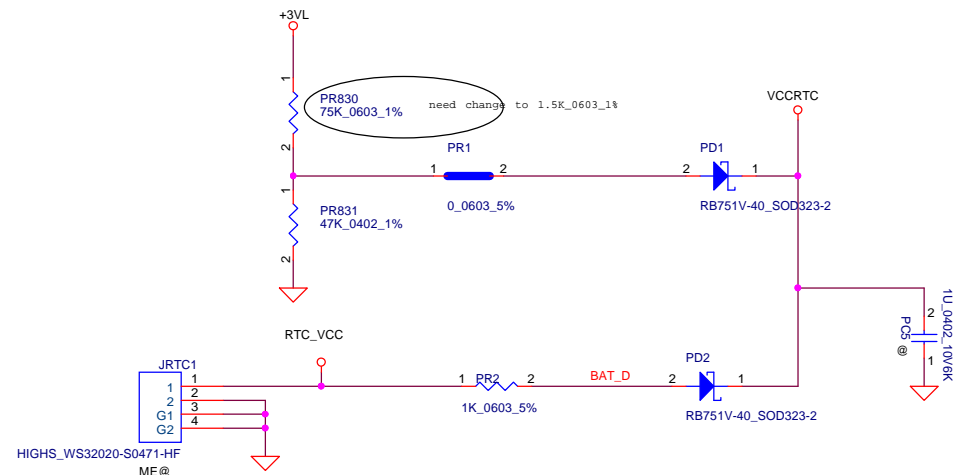
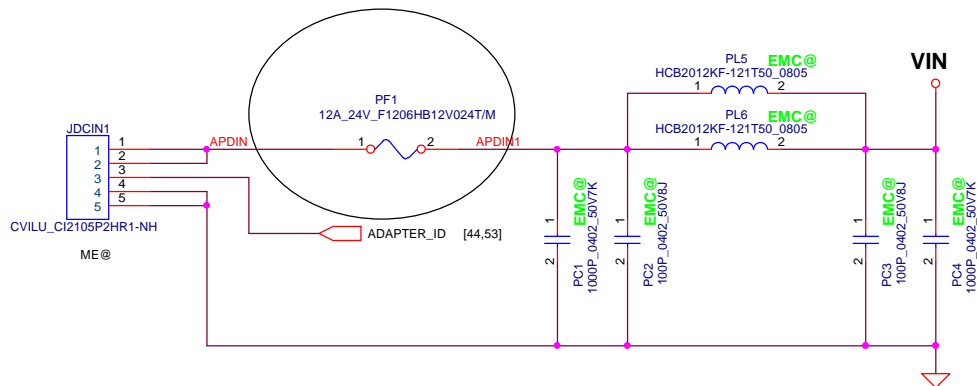



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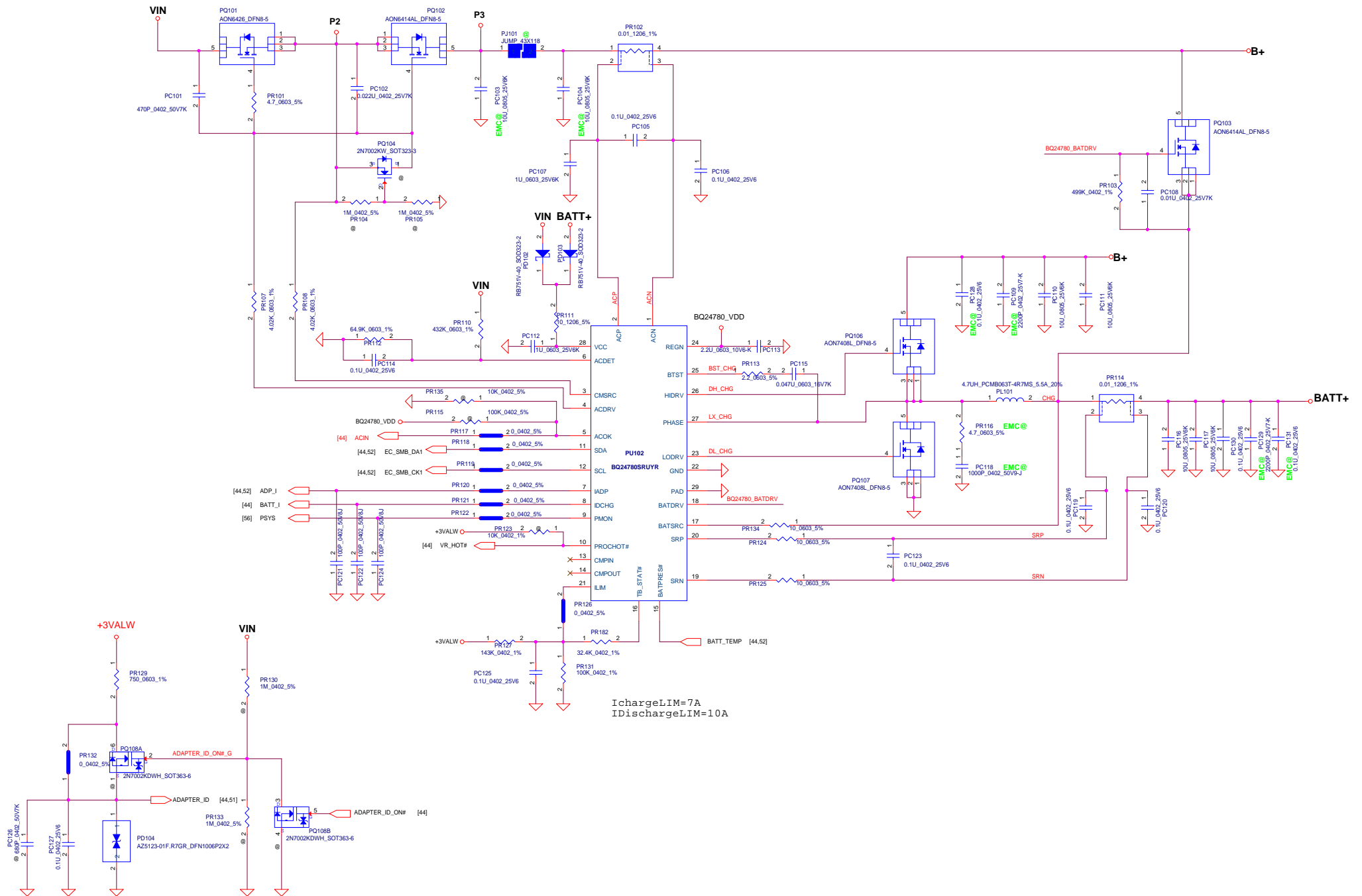
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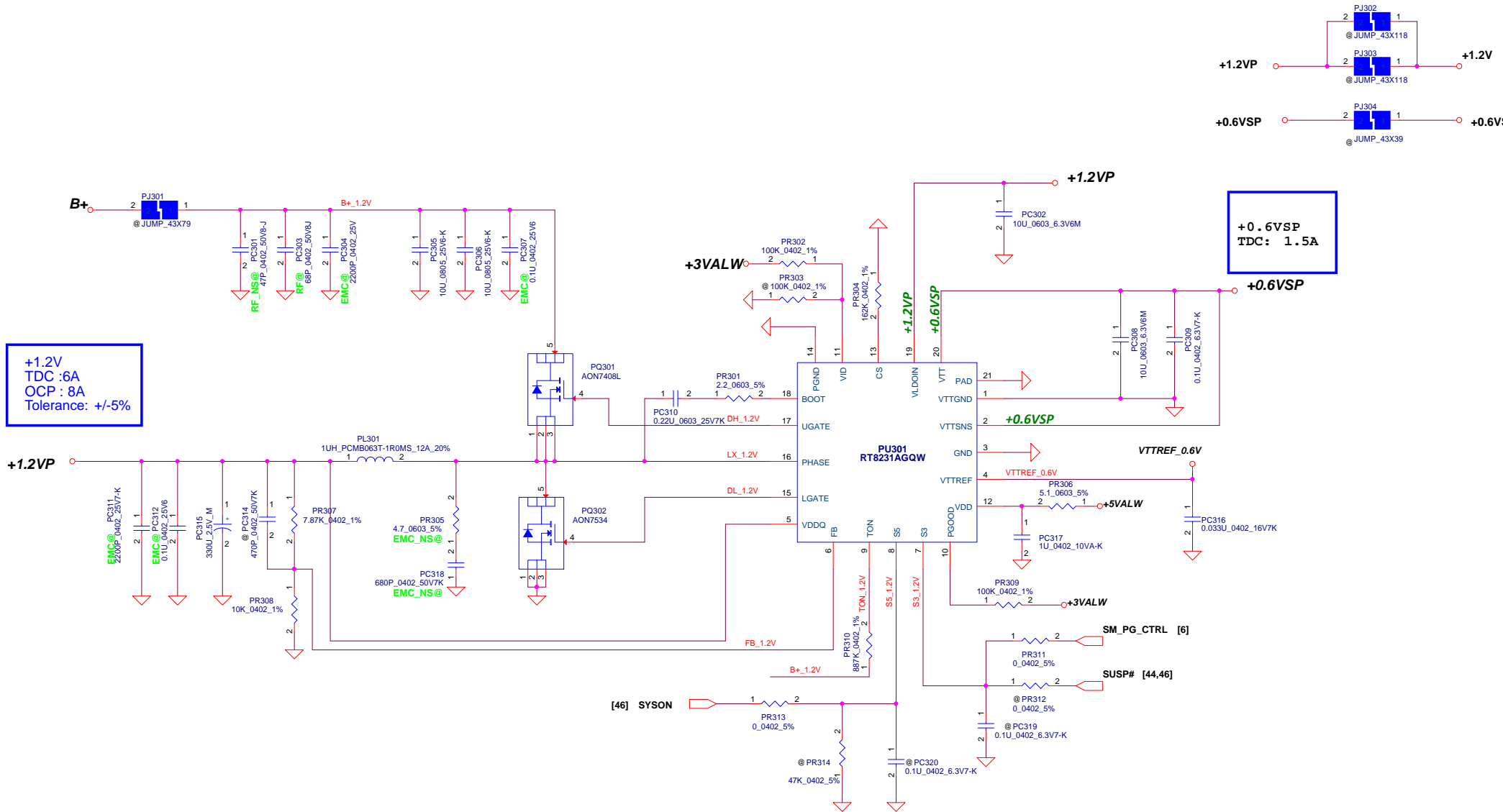




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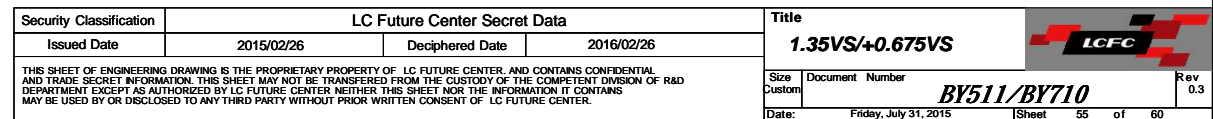
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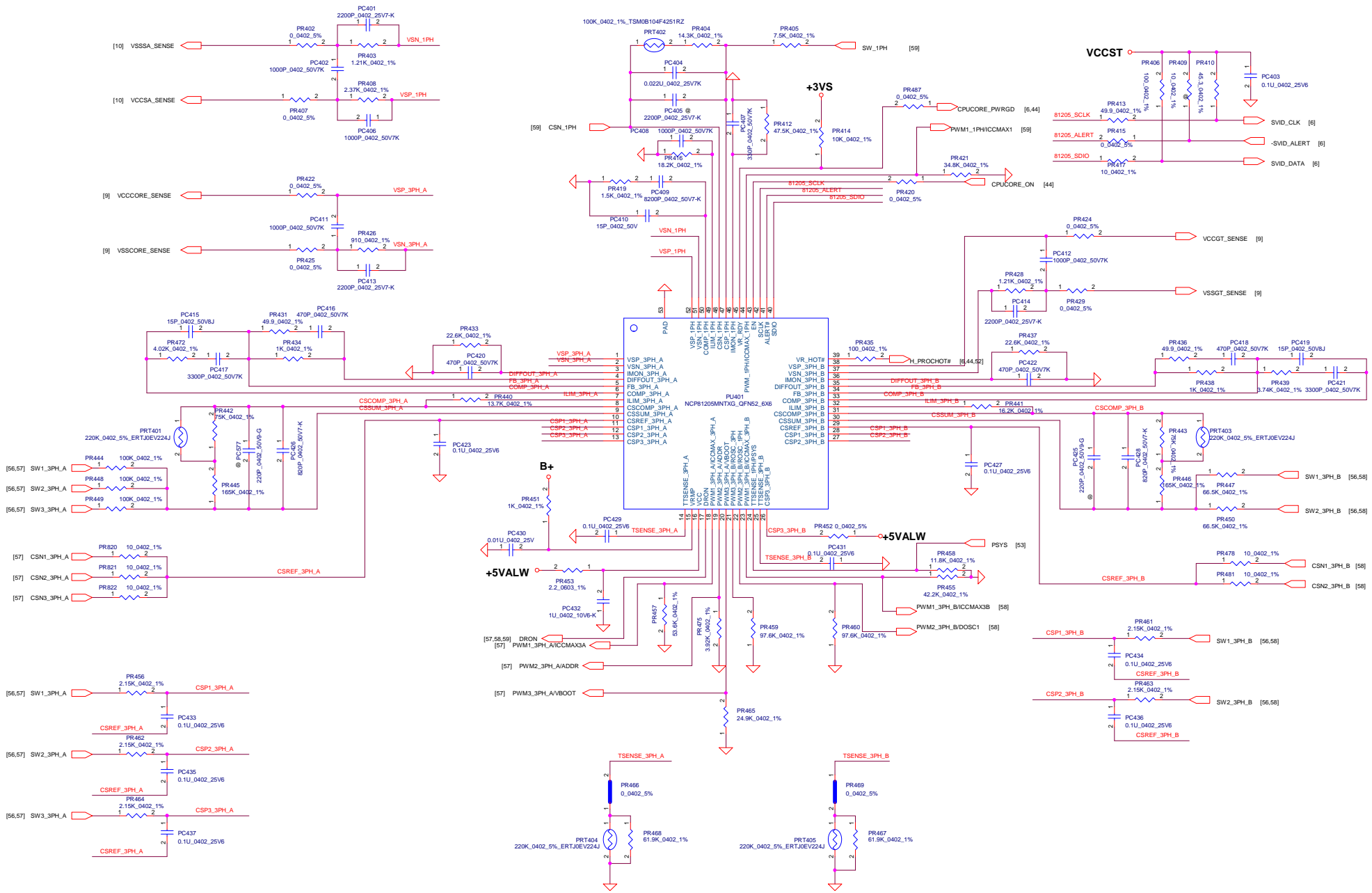
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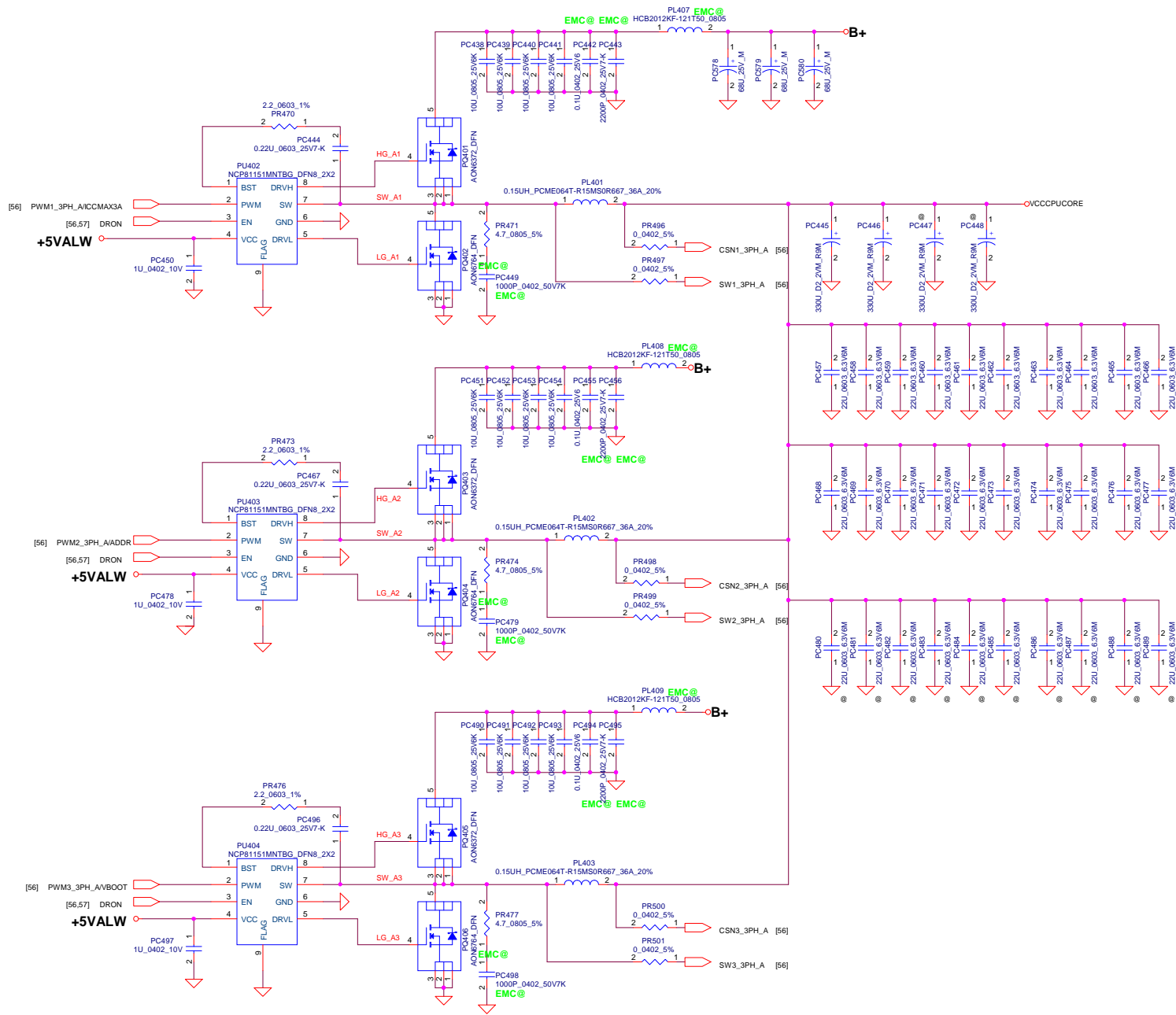
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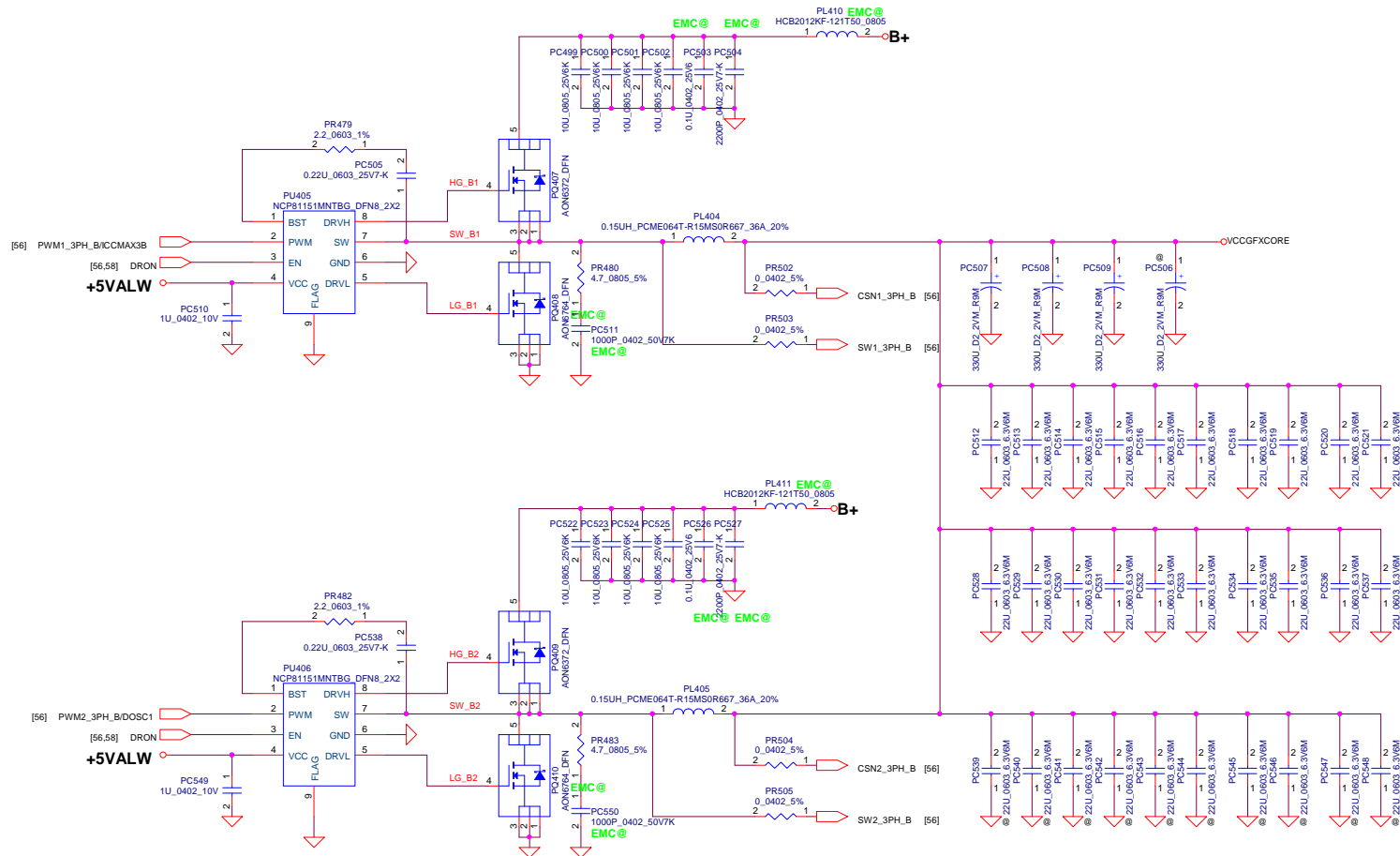
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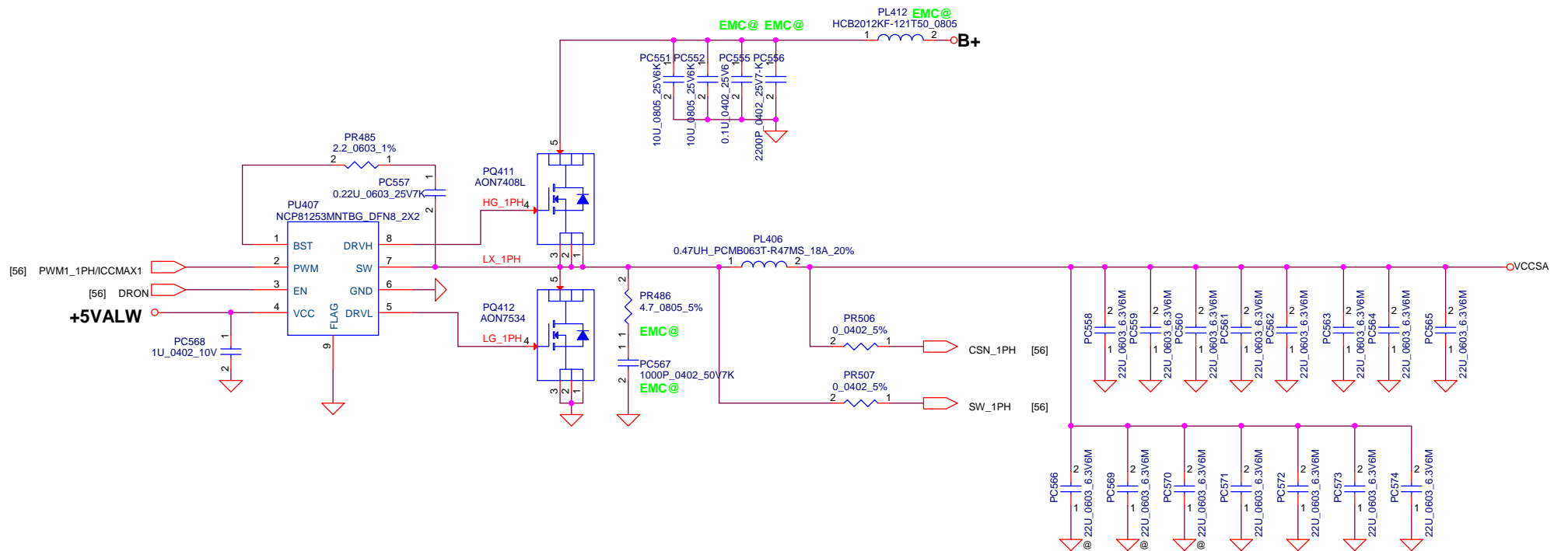





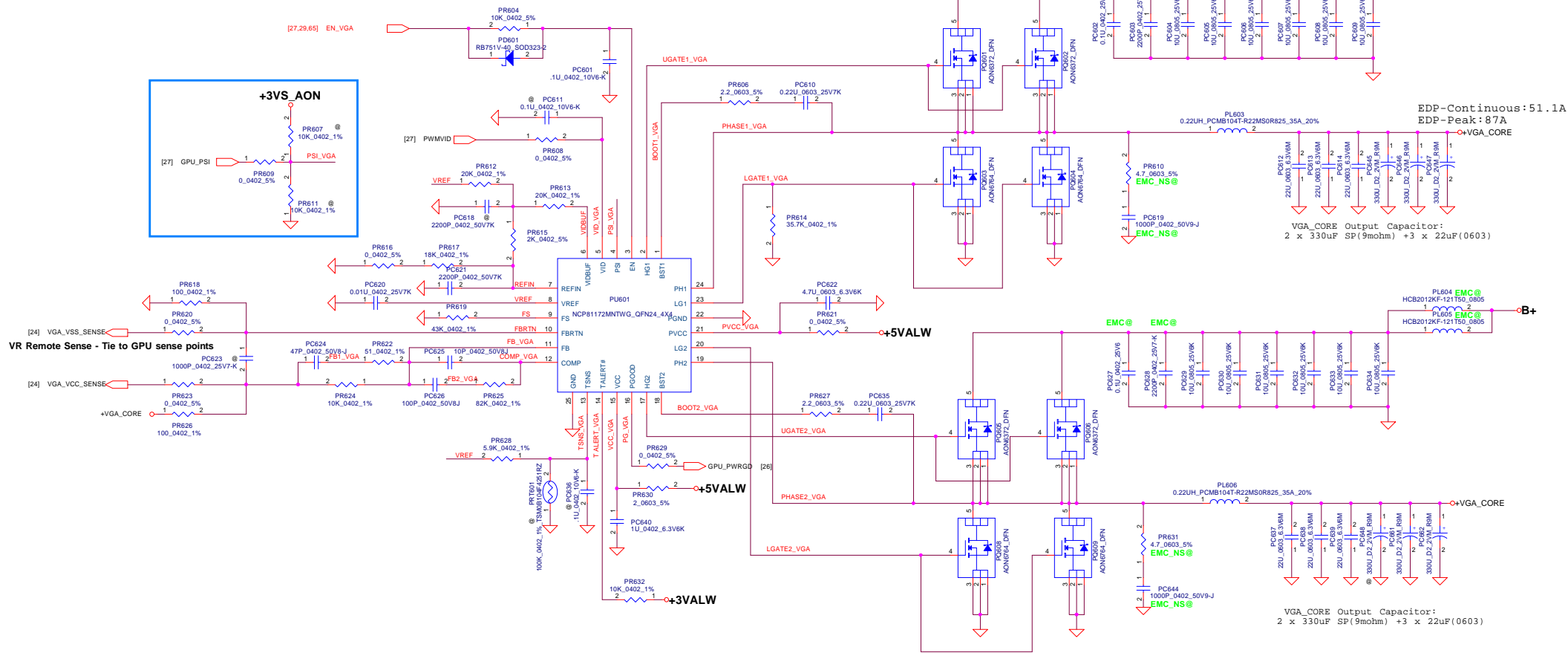






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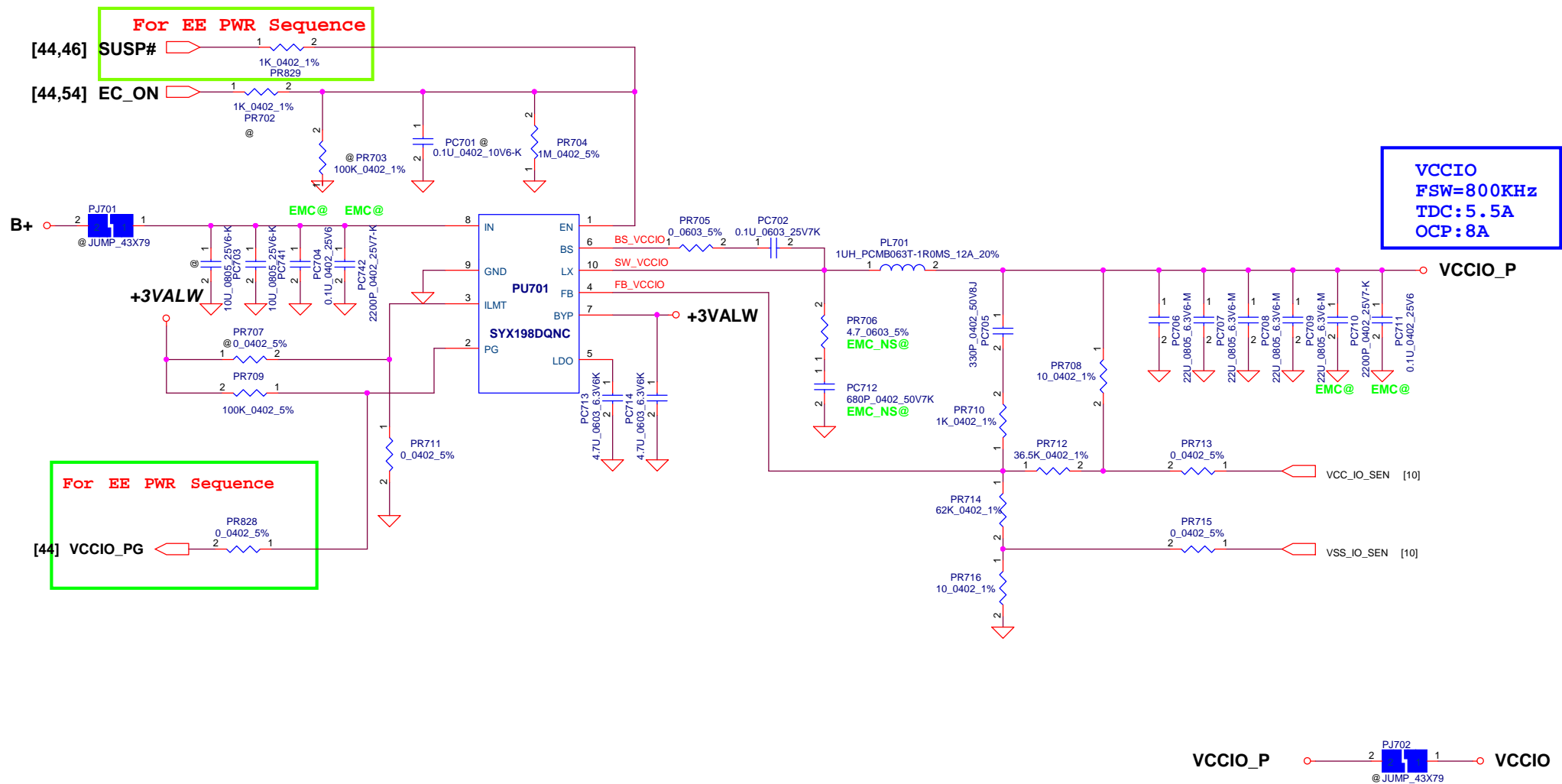



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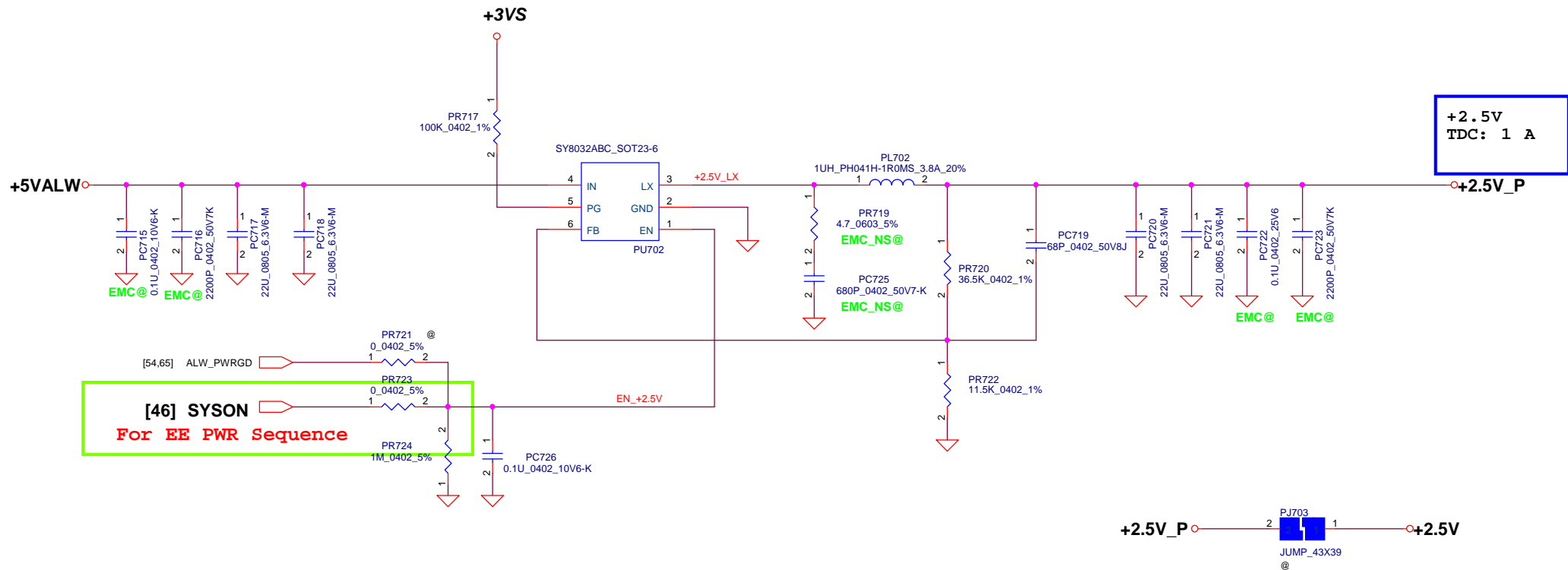
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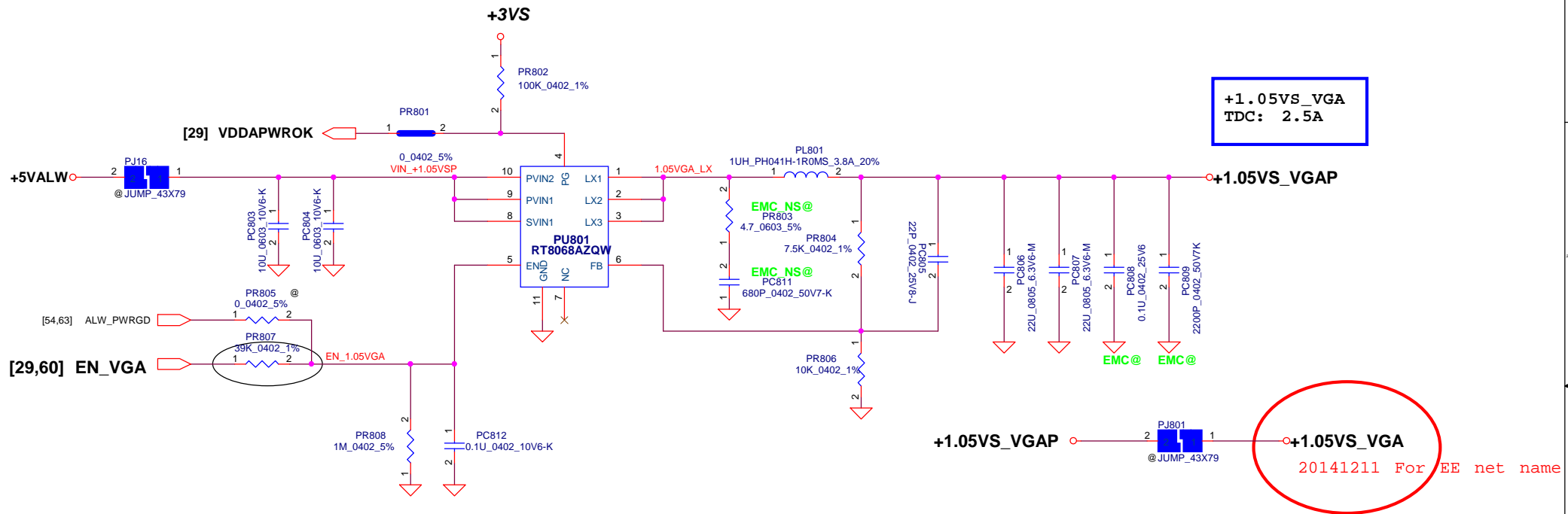
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